DIGITAL-LOGIC
smart embedded computers

Detailed Technical USER MANUAL FOR:

smartModule
SM800PC/X
SM900PC/X

Nordstrasse 11/F
CH - 4542 Luterbach
Tel.: ++41 (0)32 681 58 00
Fax: ++41 (0)32 681 58 01
Email: support@digitallogic.com
Homepage: http://www.digitallogic.com

CE

For internal use only:
File: SM800-900PCX_Detailed_V2.0E.doc
Path: R:\HANDBUCH\smart\SM800-900\SM800-900PCX_Detailed_V2.0E.doc

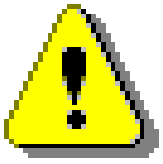
About this Manual and How to Use It

This manual is written for the original equipment manufacturer (OEM) who plans to build computer systems based on the single board MICROSPACE-PC. It is for integrators and programmers of systems based on the MICROSPACE-Computer family. This manual provides instructions for installing and configuring the board, and describes the system and setup requirements. This document contains information on hardware requirements, interconnections, and details of how to program the system. Please check the Product CD for further information and manuals.

DIGITAL-LOGIC AG offers all schematics as a design guide only. DIGITAL-LOGIC AG assumes no responsibility for final system design. It is also assumed, that the designer has the reference manual of the PENTIUM/GEODE chip, the programmers reference from the GEODE chip. DIGITAL-LOGIC AG assumes that the designer of a smartModule-800PCX design has the knowledge of designing ISA/PCI based PC architecture.

REVISION HISTORY:

Document Version	Date/Initials:	Modification: Remarks, News, Attention:
V0.1	06.2006 WAM	Initial Version
V0.2	07.2006 MEG	First Revision
V0.3	07.2006 DAR	Preliminary Version
V0.4	10.2006 DAR	Preliminary Version
V0.5	03.2007 DAR	Preliminary Version
V0.6	03.2007 DAR	Preliminary Version / SM800 BUS
V0.7	04.2007 KUF/WAS	Details fine-tuned/Standard format w/English applied
V0.8	05.2007 WAS/DAR KUF	Revision History format change / Filename & Path moved Bus on Versions 1.x & 2.x / Battery info in Timers & Clocks
V0.9	05.2007 KUF	Sections 6.6 to 6.17 – major rework
V1.0	02.2008 KUF	New Thermal Specifications Sect. 6.5 / Integration SM900PC/X
V2.0	06.2008 DAR	DesignIN Information removed -> use SM800DK Manual
V2.0A	08.2008 WAS	Power Mgmt Specs updated
V2.0B	11.2008 WAS	J1 & J2 referred to at X200 connector
V2.0C	11.2008 KUF	PCI Table added (Chapter 3.6)
V2.0D	11.2008 WAS	Operating System chapter removed (in BIOS manual)
V2.0E	***02.2009 WAS/MEG***	***Connector X200.A Pins 81-120 updated***



Attention!
1. All information in this manual, and the product, are subject to change without prior notice.
2. Read this manual prior to installation of the product.
3. Read the security information carefully prior to installation of the product.

Table of Contents

1. PREFACE

The information contained in this manual has been carefully checked and is believed to be accurate; it is subject to change without notice. Product advances mean that some specifications may have changed. DIGITAL-LOGIC AG assumes no responsibility for any inaccuracies, or the consequences thereof, that may appear in this manual. Furthermore, DIGITAL-LOGIC AG does not accept any liability arising from the use or application of any circuit or product described herein.

1.1. Trademarks

DIGITAL-LOGIC, DIGITAL-LOGIC-Logo, MICROSPACE, and smartModule are registered trademarks owned worldwide by DIGITAL-LOGIC AG, Luterbach (Switzerland). In addition, this document may include names, company logos, and registered trademarks which are, therefore, proprietary to their respective owners.

1.2. Disclaimer

DIGITAL-LOGIC AG makes no representations or warranties with respect to the contents of this manual, and specifically disclaims any implied warranty of merchantability or fitness, for any particular purpose. DIGITAL-LOGIC AG shall, under no circumstances, be liable for incidental or consequential damages or related expenses resulting from the use of this product, even if it has been notified of the possibility of such damage.

1.3. Environmental Protection Statement

This product has been manufactured to satisfy environmental protection requirements wherever possible. Many of the components used (structural parts, printed circuit boards, connectors, batteries, etc.) are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

1.4. Who should use this Product

- Electrical engineers with know-how in PC-technology.
- Because of the complexity and the variability of PC-technology, we cannot guarantee that the product will work in any particular situation or set-up. Our technical support will try to help you find a solution.
- Pay attention to electrostatic discharges; use a CMOS protected workplace.
- Power supply must be OFF when working on the board or connecting any cables or devices.

1.5. Recycling Information

All components within this product fulfill the requirements of the RoHS (Restriction of Hazardous Substances Directive). The product is soldered with a lead free process.

1.6. Technical Support

1. Contact your local DIGITAL-LOGIC Technical Support, in your country.
2. Use the Internet Support Request form at http://support.digitallogic.ch/ → embedded products → New Support Request

Support requests are only accepted with detailed information about the product (i.e., BIOS-, Board-version)!

1.7. Limited Two Year Warranty

DIGITAL-LOGIC AG guarantees the hardware and software products it manufactures and produces to be free from defects in materials and workmanship for two years following the date of shipment from DIGITAL-LOGIC AG, Switzerland. This warranty is limited to the original purchaser of the product and is not transferable.

During the two year warranty period, DIGITAL-LOGIC AG will repair or replace, at its discretion, any defective product or part at no additional charge, provided that the product is returned, shipping prepaid, to DIGITAL-LOGIC AG. All replaced parts and products become property of DIGITAL-LOGIC AG.

Before returning any product for repair, direct customers of DIGITAL-LOGIC AG, Switzerland are required to register a RMA (Return Material Authorization) number in the Support Center at http://support.digitallogic.ch/

All other customers must contact their local distributors for returning defective materials.

This limited warranty does not extend to any product which has been damaged as a result of accident, misuse, abuse (such as use of incorrect input voltages, wrong cabling, wrong polarity, improper or insufficient ventilation, failure to follow the operating instructions that are provided by DIGITAL-LOGIC AG or other contingencies beyond the control of DIGITAL-LOGIC AG), wrong connection, wrong information or as a result of service or modification by anyone other than DIGITAL-LOGIC AG. Nor if the user has insufficient knowledge of these technologies or has not consulted the product manuals or the technical support of DIGITAL-LOGIC AG and therefore the product has been damaged.

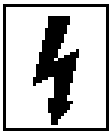
Empty batteries (external and onboard), as well as all other battery failures, are not covered by this manufacturer's limited warranty.

Except, as directly set forth above, no other warranties are expressed or implied, including, but not limited to, any implied warranty of merchantability and fitness for a particular purpose, and DIGITAL-LOGIC AG expressly disclaims all warranties not stated herein. Under no circumstances will DIGITAL-LOGIC AG be liable to the purchaser or any user for any damage, including any incidental or consequential damage, expenses, lost profits, lost savings, or other damages arising out of the use or inability to use the product.

1.8. Explanation of Symbols

CE Conformity
This symbol indicates that the product described in this manual is in compliance with all applied CE standards.

Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 60V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment.



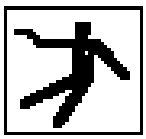
Caution, Electric Shock!
This symbol and title warn of hazards due to electrical shocks (> 32V) when touching products or parts of them. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your equipment

Warning, ESD Sensitive Device!
This symbol and title inform that electronic boards and their components are sensitive to Electro Static Discharge (ESD). In order to ensure product integrity at all times, care must always be taken while handling and examining this product.

Attention!
This symbol and title emphasize points which, if not fully understood and taken into consideration by the reader, may endanger your health and/or result in damage to your equipment.

Note...
This symbol and title emphasize aspects the user should read through carefully for his, or her, own advantage.

Warning, Heat Sensitive Device!
This symbol indicates a heat sensitive component.



Safety Instructions
This symbol shows safety instructions for the operator to follow.

This symbol warns of general hazards from mechanical, electrical, and/or chemical failure. This may endanger your life/health and/or result in damage to your equipment.

1.9. Applicable Documents and Standards

The following publications are used in conjunction with this manual. When any of the referenced specifications are superseded by an approved revision, that revision shall apply. All documents may be obtained from their respective organizations.

- Advanced Configuration and Power Interface Specification Revision 2.0c, August 25, 2003 Copyright © 1996-2003 Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Ltd., Toshiba Corporation. All rights reserved. http://www.acpi.info/
- ANSI/TIA/EIA-644-A-2001: Electrical Characteristics of Low Voltage Differential Signaling (LVDS) Interface Circuits, January 1, 2001. http://www.ansi.org/
- ANSI INCITS 361-2002: AT Attachment with Packet Interface - 6 (ATA/ATAPI-6), November 1, 2002. http://www.ansi.org/
- ANSI INCITS 376-2003: American National Standard for Information Technology – Serial Attached SCSI (SAS), October 30, 2003. http://www.ansi.org/
- Audio Codec '97 Revision 2.3 Revision 1.0, April 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://www.intel.com/labs/media/audio/
- Display Data Channel Command Interface (DDC/CI) Standard (formerly DDC2Bi) Version 1, August 14, 1998 Copyright © 1998 Video Electronics Standards Association. All rights reserved. http://www.vesa.org/summary/sumddcci.htm
- ExpressCard Standard Release 1.0, December 2003 Copyright © 2003 PCMCIA. All rights reserved. http://www.expresscard.org/
- IEEE 802.3-2002, IEEE Standard for Information technology, Telecommunications and information exchange between systems–Local and metropolitan area networks–Specific requirements – Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications. http://www.ieee.org
- IEEE 802.3ae (Amendment to IEEE 802.3-2002), Part 3: Carrier Sense Multiple Access with Collision Detection (CSMA/CD) Access Method and Physical Layer Specifications, Amendment: Media Access Control (MAC) Parameters, Physical Layers, and Management Parameters for 10 GB/s Operation. http://www.ieee.org
- Intel Low Pin Count (LPC) Interface Specification Revision 1.1, August 2002 Copyright © 2002 Intel Corporation. All rights reserved. http://developer.intel.com/design/chipsets/industry/lpc.htm
- PCI Express Base Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Express Card Electromechanical Specification Revision 1.1, March 28, 2005, Copyright © 2002-2005 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI Local Bus Specification Revision 2.3, March 29, 2002 Copyright © 1992, 1993, 1995, 1998, 2002 PCI Special Interest Group. All rights reserved. http://www.pcisig.com/
- PCI-104 Specification, Version V1.0, November 2003. All rights reserved. http://www.pc104.org
- PICMG® Policies and Procedures for Specification Development, Revision 2.0, September 14, 2004, PCI Industrial Computer Manufacturers Group (PICMG®), 401 Edgewater Place, Suite 500, Wakefield, MA 01880, USA, Tel: 781.224.1100, Fax: 781.224.1239. http://www.picmg.org/
- Serial ATA: High Speed Serialized AT Attachment Revision 1.0a January 7, 2003 Copyright © 2000-2003, APT Technologies, Inc, Dell Computer Corporation, Intel Corporation, Maxtor Corporation, Seagate Technology LLC. All rights reserved. http://www.sata-io.org/

- Smart Battery Data Specification Revision 1.1, December 11, 1998. www.sbs-forum.org
- System Management Bus (SMBus) Specification Version 2.0, August 3, 2000 Copyright © 1994, 1995, 1998, 2000 Duracell, Inc., Energizer Power Systems, Inc., Fujitsu, Ltd., Intel Corporation, Linear Technology Inc., Maxim Integrated Products, Mitsubishi Electric Semiconductor Company, Power-Smart, Inc., Toshiba Battery Co. Ltd., Unitrode Corporation, USAR Systems, Inc. All rights reserved. http://www.smbus.org/
- Universal Serial Bus Specification Revision 2.0, April 27, 2000 Copyright © 2000 Compaq Computer Corporation, Hewlett-Packard Company, Intel Corporation, Lucent Technologies Inc., Microsoft Corporation, NEC Corporation, Koninklijke Philips Electronics N.V. All rights reserved. http://www.usb.org/

1.10. For Your Safety

Your new DIGITAL-LOGIC product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long, fault-free life. However, this life expectancy can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and for the correct operation of your new DIGITAL-LOGIC product, please comply with the following guidelines.

Attention!
All work on this device must only be carried out by sufficiently skilled personnel.

Caution, Electric Shock!
Before installing your new DIGITAL-LOGIC product, always ensure that your mains power is switched off. This applies also to the installation of piggybacks or peripherals. Serious electrical shock hazards can exist during all installation, repair and maintenance operations with this product. Therefore, always unplug the power cable and any other cables which provide external voltage before performing work.

Warning, ESD Sensitive Device!
Electronic boards and their components are sensitive to static electricity. In order to ensure product integrity at all times, be careful during all handling and examinations of this product.

1.11. RoHS Commitment

DIGITAL-LOGIC AG is committed to develop and produce environmentally friendly products according to the Restriction of Hazardous Substances (RoHS) Directive (2002/95/EC) and the Waste Electrical and Electronic Equipment (WEEE) Directive (2002/96/EC) established by the European Union. The RoHS directive was adopted in February 2003 by the European Union and came into effect on July 1, 2006. It is not a law but a directive, which restricts the use of six hazardous materials in the manufacturing of various types of electronic and electrical equipment. It is closely linked with the Waste Electrical and Electronic Equipment Directive (WEEE) 2002/96/EC, which has set targets for collection, recycling and recovery of electrical goods and is part of a legislative initiative to solve the problem of huge amounts of toxic e-waste.

Each European Union member state is adopting its own enforcement and implementation policies using the directive as a guide. Therefore, there could be as many different versions of the law as there are states in the EU. Additionally, non-EU countries like China, Japan, or states in the U.S. such as California may have their own regulations for green products, which are similar, but not identical, to the RoHS directive.

RoHS is often referred to as the "lead-free" directive but it restricts the use of the following substances:

- Lead
- Mercury
- Cadmium
- Chromium VI
- PBB and PBDE

The maximum allowable concentration of any of the above mentioned substances is 0.1% (except for Cadmium, which is limited to 0.01%) by weight of homogeneous material. This means that the limits do not apply to the weight of the finished product, or even to a component but to any single substance that could (theoretically) be separated mechanically.

1.11.1. RoHS Compatible Product Design

All DIGITAL-LOGIC standard products comply with RoHS legislation.

Since July 1, 2006, there has been a strict adherence to the use of RoHS compliant electronic and mechanical components during the design-in phase of all DIGITAL-LOGIC standard products.

1.11.2. RoHS Compliant Production Process

DIGITAL-LOGIC selects external suppliers that are capable of producing RoHS compliant devices. These capabilities are verified by:

1. A confirmation from the supplier indicating that their production processes and resulting devices are RoHS compliant.
2. If there is any doubt of the RoHS compliancy, the concentration of the previously mentioned substances in a produced device will be measured. These measurements are carried out by an accredited laboratory.

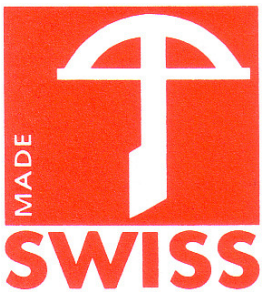
1.11.3. WEEE Application

The WEEE directive is closely related to the RoHS directive and applies to the following devices:

- Large and small household appliances
- IT equipment
- Telecommunications equipment (although infrastructure equipment is exempt in some countries)
- Consumer equipment
- Lighting equipment – including light bulbs
- Electronic and electrical tools
- Toys, leisure and sports equipment
- Automatic dispensers

It does not apply to fixed industrial plants and tools. The compliance is the responsibility of the company that brings the product to market, as defined in the directive. Components and sub-assemblies are not subject to product compliance. In other words, since DIGITAL-LOGIC does not deliver ready-made products to end users the WEEE directive is not applicable for DIGITAL-LOGIC. Users are nevertheless encouraged to properly recycle all electronic products that have reached the end of their life cycle.

1.12. Swiss Quality



- 100% Made in Switzerland
- DIGITAL-LOGIC is a member of "Swiss-Label"
- This product was ***not*** manufactured by employees earning piecework wages
- This product was manufactured in humane work conditions
- All employees who worked on this product are paid customary Swiss market wages and are insured
- ISO 9000:2001 (quality management system)

1.13. The Swiss Association for Quality and Management Systems

The Swiss Association for Quality and Management Systems (SQS) provides certification and assessment services for all types of industries and services. SQS certificates are accepted worldwide thanks to accreditation by the Swiss Accreditation Service (SAS), active membership in the International Certification Network, IQNet, and co-operation contracts/agreements with accredited partners.

www.sqs.ch

The SQS Certificate ISO 9001:2000 has been issued to DIGITAL-LOGIC AG, the entire company, in the field of development, manufacturing and sales of embedded computer boards, embedded computer modules and computer systems. The certification is valid for three years at which time an audit is performed for recertification.

2. OVERVIEW

2.1. Standard Features

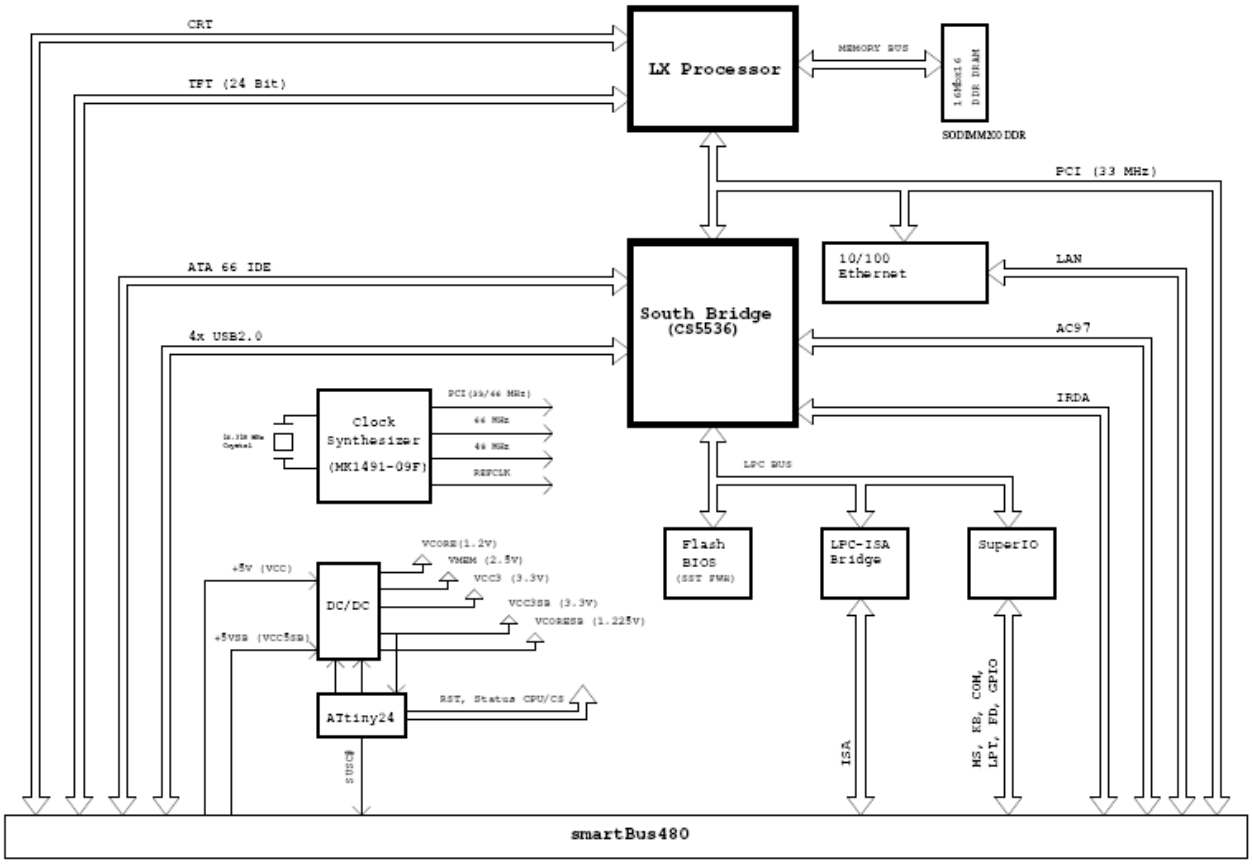
The smartModule-800PCX is a miniaturized PC on-chip unit incorporating the major elements of a PC/AT compatible computer. It includes standard PC/AT compatible elements, such as:

- Powerful AMD Geode LX800 core or AMD Geode LX900 core
- BIOS FLASH
- SODIMM socket for 256-1024MB
- Timers
- DMA
- Real-time clock
- 2k EEPROM
- LPT1
- COM1 (TTL), COM2 (TTL)
- Speaker interface
- AT-keyboard interface
- PS/2 mouse interface
- Floppy disk interface
- 1x ATA-IDE hard disk interface
- VGA/LCD video controller
- Embedded smartBUS480
- 3.3V power supply (switched mode)

2.2. Unique Features

- EEPROM for setup and configuration
- UL approved parts
- AC97 audio bus
- 2x additional USB 2.0 port

2.3. SM800PC/X SM900PC/X Block Diagram



2.4. Specifications

CPU	Specification
CPU	AMD GEODE LX800 / LX900
Mode	Real / Protected
Compatibility	8086 - 80586
First Level Cache	128kB write-back
Word Size	32bits
Physical Addressing	32 lines
Clock Rates	500MHz / 600MHz

Math Coprocessor	Specification
	Available on the CPU

Power Management	Specification
	The LX800/LX900 supports ACPI and APM Version 1.2 The following ACPI Sleep States are supported: ➢ S1 (Standby) ➢ S3 (Suspend to RAM) not available ➢ S4 (Hibernation)

DMA	Specification
8237A comp.	4 channel 8bit

Interrupts	Specification
8259 comp.	8 + 7 levels
	PC compatible

Timers	Specification
8254 comp.	3 programmable counters/timers

Memory	Specification
DRAM	SODIMM200pin holder for: DDR PC2700 333MHz (256-1024MByte)

Video	Specification
Controller	GEODE LX800 / LX900 graphics
CRT	2-254MByte up to 1920x1440
LCD	Up to 1600x1200
Panel	18/24bit
Drivers	For CRT only, Panel only or simultaneous CRT and Panel: WIN2000, XP

Mass Storage	Specification
FD	Floppy disk interface, for max. 1 floppy
HD	1-IDE interface, AT-type, for max. 2 hard disks

Standard AT Interfaces	Specification					
Serial	Name	FIFO	IRQs	Addr.	Signals	Remarks
	COM1 COM2	yes yes	IRQ4 IRQ3	3F8 2F8		
	(Baud rates: 50-115KBaud programmable)					
Parallel	LPT1 printer interface, Modes: SPP (output), EPP (bidir.), ECP (Centronics)					
Keyboard	AT or PS/2 keyboard					
Mouse	PS/2					
Speaker	External 0.1W output drive					
RTC	Integrated into the CS5536 with CMOS-RAM 256Byte					
Backup current	<5 µA at 3V					
Battery	External 3Volt Lithium					

Supervisory	Specification
Watchdog	Integrated in W83627 Super-IO, strobe time max. 1 sec.

BUS	Specification
ISA	Compatible with restrictions
ISA-Clock	14.318MHz
PCI/104plus	IEEE-996 standard bus, buffered
PCI-Clock	33MHz
USB V2.0	4x
Ext. DDR-DRAM-Bus	Not available

Power Supply	Specification
Working	5Volt ± 5%, 3.3V onboard switch mode regulator
Power Rise Time	> 100µs (0V ➔ 4.75V)

Physical Characteristics	Specification
Dimensions	Length: 85 mm +/- 0.1mm Depth: 66 mm +/- 0.1mm Height: 16 mm +/- 0.2mm (with 5mm bus connectors)
Weight	90g (9 oz)
PCB Thickness	1.6mm (0.0625 inches nominal)
PCB Layer	Multilayer

Operating Environment	Specification
Relative humidity	5-90%, non-condensing
Vibration	To be tested
Shock	To be tested
Temperature	Operating: Standard version: -25°C to +70°C Extended version: -40°C to +85°C Storage: -55°C to +85°C

EMI/EMC (IEC1131-2 refer MIL 461/462)	Specification
 ESD Electro Static Discharge:	IEC 801-2, EN55101-2, VDE 0843/0847 Part 2 Metallic protection needed Separate ground layer included 15kV single peak
REF Radiated Electromagnetic Field:	IEC 801-3, VDE 0843 Part 3, IEC770 6.2.9. Not tested
EFT Electric Fast Transient (Burst):	IEC 801-4, EN50082-1, VDE 0843 Part 4 250V - 4kV, 50 ohms, Ts=5ns Grade 2: 1kV Supply, 500 I/O, 5kHz
SIR Surge Immunity Requirements:	IEC 801-5, IEEE587, VDE 0843 Part 5 Supply: 2kV, 6 pulse/minute I/O: 500V, 2 pulse/minute FD, CRT: none
High-frequency Radiation:	EN55022

All information is subject to change without notice.

2.5. Differences to the SMP5PC & SMP3PC

CPU	SM800PC/X SM900PC/X	SM520PC	Pentium I	Pentium III
CPU-Clock	**500MHz / 600MHz**	**133Mhz**	**166-266Mhz**	**300-500Mhz**
Power consumption	**6Watt**	**3-5Watt**	**5-7Watt**	**7-9Watt**
Standard functions				
Ext. DRAM Expansion	None	32bit	64bit	64bit
Keyboard & Mouse	Yes	Yes	Yes	Yes
COM1	Yes	Yes	Yes	Yes
COM2	Yes	Yes	Yes	Yes
Floppy disk	Yes	Yes	Yes	Yes
LPT1	Yes	Yes	Yes	Yes
Primary-IDE	Yes	Yes	Yes	Yes
Secondary-IDE	No	Yes	Yes	Yes
ISA-Bus	Yes *	Yes	Yes	Yes
CRT-VGA Signals	Yes	Yes	Yes	Yes
LCD 24bit	Yes	Yes	Yes	Yes
Unique functions:				
LAN	Yes (SM800PCX or SM900PCX)	No	No	No
PCI-Bus	Yes	Yes	Yes	Yes
36bit LCD Extension	No	Yes	Yes	Yes
USB Interface	Yes, 4ch, V2.0	No	Yes, 2ch, V1.1	Yes, 2ch, V1.1
AC97 Sound	Yes	No	No	No
Video Input Port	Yes 16bit	No	No	No
LPC-Bus	Yes	No	No	No
Serial Bus	Yes	No	No	No

* please refer to section 2.6.1.

New functions/signals on the sm480bus:

The following additional functions/signals are connected on the DRAM-signals on the sm480bus, which is not available on the SM800PCX product.

- AC97-Bus to connect a CODEC for 5.1. Sound
- Additional (USB V2.0) USB3 and USB4
- Video Input Port
- LAN-LED's
- LPC-Bus
- Serial Bus

2.6. SM800PC/X & SM900PC/X Incompatibilities to a Standard PC/AT

2.6.1. PC104 BUS / ISA BUS on SM800PC/X Version 1.x

An onboard LPC to ISA-bridge makes it possible to expand the functionality of the board with additional PC/104 cards.

Unfortunately, because of the transformation from LPC to ISA it is not possible to realize a 16bit access. This does not mean that these cards cannot be used, but that the 16bit access is divided into two. Therefore the access to these cards is a little bit slower.

The LPC support the following bus cycles:

Cycle Type	Sizes Supported	Comments
Memory Read	1Byte	Optional for both LPC hosts and peripherals
Memory Write	1Byte	Optional for both LPC hosts and peripherals.
I/O Read	1Byte	Optional for peripherals.
I/O Write	1Byte	Optional for peripherals.
DMA Read	1, 2, 4Byte	Optional for peripherals.
DMA Write	1, 2, 4Byte	Optional for peripherals.
Bus Master Memory Read	1, 2, 4Byte	Optional for both LPC hosts and peripherals, but strongly recommended for hosts.
Bus Master Memory Write	1, 2, 4Byte	Optional for both LPC hosts and peripherals, but strongly recommended for hosts.
Bus Master I/O Read	1, 2, 4Byte	Optional for both LPC hosts and peripherals.
Bus Master I/O Write	1, 2, 4Byte	Optional for both LPC hosts and peripherals.
Firmware Memory Read	1, 2, 4, 128Byte	Optional for both LPC hosts and peripherals.
Firmware Memory Write	1, 2, 4Byte	Optional for both LPC hosts and peripherals.

This means, all Non-BusMaster I/O and MEM Cycles are only 8bit wide and never 16bit wide. 16bit data transfer is available in the BusMaster modus only.

2.6.2. SM800PC/X Version 2.x

No incompatibilities are known. The ISA-Bus is generated from the PCI-bridge.

2.6.3. SM900PC/X

No incompatibilities are known. The ISA-Bus is generated from the PCI-bridge.

2.7. Ordering Codes

805212 SM800PCX	smartModule-800PCX, 500MHz, 0MB, LAN
805210 SM800PC	smartModule-800PC, 500MHz, 0MB
805220 SM800DK	smartDevelopment-Kit
805242 SM900PCX	smartModule-900PCX, 600MHz, 0MB, LAN
805244 SM900pc	smartModule-900PC, 600MHz, 0MB
805250 sm900dk	smartDevelopment-Kit

These are only examples; for current ordering codes, please see the current price list.

2.8. Related Application Notes

Application Notes are available at *http://www.digitallogic.com* ➔ support, or on any DIGITAL-LOGIC Application CD.

#	Description

3. PC FUNCTIONAL DESCRIPTION

3.1. Interrupt Controllers

An 8259A compatible interrupt controller, within the Geode chipset, provides seven prioritized interrupt levels. Of these, several are normally associated with the board's onboard device interfaces and controllers, and several are available on the AT expansion bus.

Interrupt:	Sources:	Onboard used:
IRQ0	ROM-BIOS clock tick function, from timer 0	yes
IRQ1	Keyboard controller output buffer full	yes
IRQ2	Used for cascade 2. 8259	yes
IRQ3	COM2 serial port	yes
IRQ4	COM1 serial port	yes
IRQ5	LPT2 parallel printer (if present)	no *
IRQ6	Floppy controller	yes
IRQ7	LPT1 parallel printer	yes
IRQ8	Battery backed clock	yes
IRQ9	Free for user	no *
IRQ10	Free for user	no *
IRQ11	Free for user	no *
IRQ12	PS/2 mouse	yes
IRQ13	Math. coprocessor	yes
IRQ14	Hard disk IDE / SCSI	yes
IRQ15	Free for user	no *

* It may depend on the LAN configuration.

3.2. Timers and Counters

3.2.1. Programmable Timers

An 8253 compatible timer/counter device is also included in the board's CS5536 device. This device is utilized in precisely the same manner as in a standard AT implementation. Each channel of the 8253 is driven by a 1.190 MHz clock, derived from a 14.318 MHz oscillator, which can be internally divided in order to provide a variety of frequencies.

Timer 2 can also be used as a general purpose timer if the speaker function is not required.

Note...
In a battery-less application, the system integrator must check the function and accuracy of the Real Time OS.

Timer Assignment

Timer	Function
0	ROM-BIOS clock tick (18.2 Hz)
1	DRAM refresh request timing (15 µs)
2	Speaker tone generation time base

3.2.2. Battery-backed Clock – Real Time Clock (RTC)

An AT compatible date/time clock is located within the chipset. The device also contains a CMOS static RAM, compatible with those in standard ATs. System configuration data is normally stored in the clock chip's CMOS RAM in a manner consistent with the convention used in other AT compatible computers.

Connect an external Lithium battery of 3.6V to the RTC pin.

The battery-backed clock can be set by using DIGITAL-LOGIC AG “SETUP” at boot-time.

Addresses:	70h =	Index register
	71h =	Data transfer register
RTC-Address MAP :	00 - 0F	Real time clock
	10 - 3F	BIOS setup (Standard)
	40 - 7F	Extended BIOS

With an external Lithium 3.6V battery, the board is able to work for over 10 years without battery replacement. The chip set consumes the following currents:

Typical battery current at 25°C:	System off	<5 µA
	System on	<1 µA

The system integrator must measure the battery current for both cases: system off and system on. With the actual measured current and the capacity of the battery, the total lifetime must be calculated.

3.2.3. Watchdog

The watchdog timer detects a system crash and performs a hardware reset. After power-up, the watchdog is always disabled as the BIOS does not send strobes to the watchdog. In case the user wants to take advantage of the watchdog, the application must produce a strobe at least every 800 ms. If no strobe occurs within the 800 ms, the watchdog resets the system.

Please refer also to the driver/software/BIOS manual “GEODE_LX800-LX900.pdf” on the Product CD, the chapter on Special Peripherals, Subsection “INT 15h SFR Functions”.

3.3. ROM-BIOS / EEPROM Memory

3.3.1. ROM-BIOS

An EPROM with 8bit wide data access normally contains the board's AT compatible ROM-BIOS. The BIOS takes an E82802A EPROM (or equivalent) device. The board's wait-state control logic automatically inserts four memory wait states in all CPU accesses to this (socket). The ROM-BIOS occupies the memory area from C0000h through FFFFFh; however, the board's ASIC logic reserves the entire area from C0000h through FFFFFh for onboard devices, so that this area is already available for ROM-DOS and BIOS expansion modules.

Consult the appropriate address map for the MICROSPACE SM800PC/X SM900PC/X ROM-BIOS.

3.3.1.1. Standard BIOS ROM

DEVICE: 82802AC-40 (SST49L008A-33-4C-EIE)

MAP: C0000h - FFFFFh Core and VGA BIOS, 1MB onboard soldered

3.3.2. EEPROM Memory for Set up

The EEPROM is used for setup and configuration data, stored as an alternative to the CMOS-RTC. Optionally, the EEPROM setup driver may update the CMOS RTC, if the battery runs down and the checksum error appears and stops the system. The capacity of the EEPROM is 2kByte.

Organization of the 2048Byte EEPROMs:

Address MAP:	Function:
0000h	**CMOS-Setup valid (01=valid)**
0001h	**Keymatrix-Setup valid (01=valid)**
0003h	**Flag for DLAG-Message (FF=no message)**
0010h-007Fh	**Copy of CMOS-Setup data**
0080h-00FFh	**Reserved for AUX-CMOS-Setup**
0100h-010Fh	**Serial-Number**
0110h-0113h	Production date (year/day/month)
0114h-0117h	1st Service date (year/day/month)
0118h-011Bh	2nd Service date (year/day/month)
011Ch-011Fh	3rd Service date (year/day/month)
0120h-0122h	Boot errors (Autoincremented if any boot error occurs)
0123h-0125h	Setup Entries (Autoincremented on every setup entry)
0126h-0128h	Low Battery (Autoincremented every time the battery is low, EEPROM -> CMOS)
0129h-012Bh	Startup (Autoincremented on every power-on start)
0130h	Number of 512k SRAM
0131h	Number of 512k Flash
0132h/0133h	BIOS Version (V1.4 => [0132h]:= 4, [0133h]:=1)
0134h/0135h	BOARD Version (V1.5 => [0124h]:=5, [0125h]:=1)
0136h	BOARD TYPE (‘M’=PC/104, ‘E’=Euro, ‘W’=MSWS, ‘S’=Slot, ‘C’=Custom)
0137h	CPU TYPE (01h=ELAN300/310, 02h=ELAN400, 03h=486SLC, 04h=486DX, 05h=P5).
0200h-03FFh	**Keymatrix-Setup data**
0200h-027Fh	Keymatrix Table
0400h-07FFh	**Free for customer use**

3.3.3. BIOS CMOS Setup

If wrong setups are memorized in the CMOS-RAM, the customer default values will be loaded after resetting the RTC/CMOS-RAM from the EEPROM. If the battery is low, it is always possible to start the system with the customer default settings values from the EEPROM.

Attention!

On the next setup pages (switch with TAB) the values for special parameters are modifiable. Normally the parameters are set correctly by DIGITAL-LOGIC AG. Be very careful in modifying any parameter since the system could crash. Some parameters are dependent on the CPU type. The cache parameter is always available, for example. So, if you select too few “wait” states, the system will not start until you reset the CMOS-RAM using the RAM-Reset jumper, but the default values are reloaded. If you are not familiar with these parameters, do not change anything*!*

3.4. CMOS RAM Map

Systems based on the industry-standard specification include a battery backed Real Time Clock chip. This clock contains at least 64Bytes of non-volatile RAM. The system BIOS uses this area to store information including system configuration and initialization parameters, system diagnostics, and the time and date. This information remains intact even when the system is powered down.

The BIOS supports 128Bytes of CMOS RAM. This information is accessible through I/O ports 70h and 71h. CMOS RAM can be divided into several segments:

- Locations 00h - 0Fh contain the real time clock (RTC) and status information
- Locations 10h - 2Fh contain system configuration data
- Locations 30h - 3Fh contain system BIOS-specific configuration data as well as chipset-specific information
- Locations 40h - 7Fh contain chipset-specific information as well as power management configuration parameters

The following table provides a summary of how these areas may be further divided.

Beginning	Ending	Checksum	Description
00h	0Fh	No	RTC and Checksum
10h	2Dh	Yes	System Configuration
2Eh	2Fh	No	Checksum Value of 10h - 2Dh
30h	33h	No	Standard CMOS
34h	3Fh	No	Standard CMOS - SystemSoft Reserved
40h	5Bh	Yes	Extended CMOS - Chipset Specific
5Ch	5Dh	No	Checksum Value of 40h - 5Bh
5Eh	6Eh	No	Extended CMOS - Chipset Specific
6Fh	7Dh	Yes	Extended CMOS - Power Management
7Eh	7Fh	No	Checksum Value of 6Fh - 7Dh

CMOS Map

Location	Description
00h	Time of day (seconds) specified in BCD
01h	Alarm (seconds) specified in BCD
02h	Time of day (minutes) specified in BCD
03h	Alarm (minutes) specified in BCD
04h	Time of day (hours) specified in BCD
05h	Alarm (hours) specified in BCD
06h	Day of week specified in BCD
07h	Day of month specified in BCD
08h	Month specified in BCD
09h	Year specified in BCD
0Ah	Status Register A Bit 7 = Update in progress Bits 6-4 = Time based frequency divider Bits 3-0 = Rate selection bits that define the periodic interrupt rate and output frequency.
0Bh	Status Register B Bit 7 = Run/Halt 0 Run 1 Halt Bit 6 = Periodic Timer 0 Disable 1 Enable Bit 5 = Alarm Interrupt 0 Disable 1 Enable Bit 4 = Update Ended Interrupt 0 Disable 1 Enable Bit 3 = Square Wave Interrupt 0 Disable 1 Enable Bit 2 = Calendar Format 0 BCD 1 Binary Bit 1 = Time Format 0 12-Hour 1 24-Hour Bit 0 = Daylight Savings Time 0 Disable 1 Enable
0Ch	Status Register C Bit 7 = Interrupt Flag Bit 6 = Periodic Interrupt Flag Bit 5 = Alarm Interrupt Flag Bit 4 = Update Interrupt Flag Bits 3-0 = Reserved
0Dh	Status Register D Bit 7 = Real Time Clock 0 Lost Power 1 Power
0Eh	CMOS Location for Bad CMOS and Checksum Flags Bit 7 = Flag for CMOS Lost Power 0 = Power OK 1 = Lost Power Bit 6 = Flag for CMOS checksum bad 0 = Checksum is valid 1 = Checksum is bad

Continued...

CMOS Map *continued...*

Location	Description
0Fh	Shutdown Code
10h	Diskette Drives Bits 7-4 = Diskette Drive A 0000 = Not installed 0001 = Drive A = 360 kB 0010 = Drive A = 1.2MB 0011 = Drive A = 720 kB 0100 = Drive A = 1.44MB 0101 = Drive A = 2.88MB Bits 3-0 = Diskette Drive B 0000 = Not installed 0001 = Drive B = 360 kB 0010 = Drive B = 1.2MB 0011 = Drive B = 720 kB 0100 = Drive B = 1.44MB 0101 = Drive B = 2.88MB
11h	Reserved
12h	Fixed (Hard) Drives Bits 7-4 = Hard Drive 0, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 19h. Bits 3-0 = Hard Drive 1, AT Type 0000 = Not installed 0001-1110 = Types 1-14 1111 = Extended drive types 16-44. See location 2Ah.
13h	Reserved
14h	Equipment Bits 7-6 = Number of Diskette Drives 00 = One diskette drive 01 = Two diskette drives 10, 11 = Reserved Bits 5-4 = Primary Display Type 00 = Adapter with option ROM 01 = CGA in 40 column mode 10 = CGA in 80 column mode 11 = Monochrome Bits 3-2 = Reserved Bit 1 = Math Coprocessor Presence 0 = Not installed 1 = Installed Bit 0 = Bootable Diskette Drive 0 = Not installed 1 = Installed
15h	Base Memory Size (in kB) - Low Byte
16h	Base Memory Size (in kB) - High Byte
17h	Extended Memory Size (in kB) - Low Byte
18h	Extended Memory Size (in kB) - High Byte
19h	Extended Drive Type - Hard Drive 0
1Ah	Extended Drive Type - Hard Drive 1

Continued...

CMOS Map *continued...*

Location	Description
1Bh	Custom and Fixed (Hard) Drive Flags Bits 7-6 = Reserved Bit 5 = Internal Floppy Disk Controller 0 = Disabled 1 = Enabled Bit 4 = Internal IDE Controller 0 = Disabled 1 = Enabled Bit 3 = Hard Drive 0 Custom Flag 0 = Disabled 1 = Enabled Bit 2 = Hard Drive 0 IDE Flag 0 = Disabled 1 = Enabled Bit 1 = Hard Drive 1 Custom Flag 0 = Disabled 1 = Enabled Bit 0 = Hard Drive 1 IDE Flag 0 = Disabled 1 = Enabled
1Ch	Reserved
1Dh	EMS Memory Size Low Byte
1Eh	EMS Memory Size High Byte
1Fh - 24h	Custom Drive Table 0 These 6 Bytes (48 bits) contain the following data: Cylinders 10bits range 0-1023 Landing Zone 10bits range 0-1023 Write Precompensation 10bits range 0-1023 Heads 8bits range 0-15 Sectors/Track 8bits range 0-254
1Fh	Byte 0 Bits 7-0 = Lower 8 bits of Cylinders
20h	Byte 1 Bits 7-2 = Lower 6 bits of Landing Zone Bits 1-0 = Upper 2 bits of Cylinders
21h	Byte 2 Bits 7-4 = Lower 4 bits of Write Precompensation Bits 3-0 = Upper 4 bits of Landing Zone
22h	Byte 3 Bits 7-6 = Reserved Bits 5-0 = Upper 6 bits of Write Precompensation
23h	Byte 4 Bits 7-0 = Number of Heads
24h	Byte 5 Bits 7-0 = Sectors Per Track
25h - 2Ah	Custom Drive Table 1 These 6 Bytes (48 bits) contain the following data: Cylinders 10bits range 0-1023 Landing Zone 10bits range 0-1023 Write Precompensation 10bits range 0-1023 Heads 8bits range 0-15 Sectors/Track 8bits range 0-254
25h	Byte 0 Bits 7-0 = Lower 8 bits of Cylinders
26h	Byte 1 Bits 7-2 = Lower 6 bits of Landing Zone Bits 1-0 = Upper 2 bits of Cylinders

Continued...

CMOS Map *continued...*

Location	Description
27h	Byte 2 Bits 7-4 = Lower 4 bits of Write Precompensation Bits 3-0 = Upper 4 bits of Landing Zone
28h	Byte 3 Bits 7-6 = Reserved Bits 5-0 = Upper 6 bits of Write Precompensation
29h	Byte 4 Bits 7-0 = Number of Heads
2Ah	Byte 5 Bits 7-0 = Sectors Per Track
2Bh	Boot Password Bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password Bits 6-0 = Calculated Password
2Ch	SCU Password Bit 7 = Enable/Disable Password 0 = Disable Password 1 = Enable Password Bits 6-0 = Calculated Password
2Dh	Reserved
2Eh	High Byte of Checksum - Locations 10h to 2Dh
2Fh	Low Byte of Checksum - Locations 10h to 2Dh
30h	Extended RAM (kB) detected by POST - Low Byte
31h	Extended RAM (kB) detected by POST - High Byte
32h	BCD Value for Century
33h	Base Memory Installed Bit 7 = Flag for Memory Size 0 = 640kB 1 = 512kB Bits 6-0 = Reserved
34h	Minor CPU Revision Differentiates CPUs within a CPU type (i.e., 486SX vs 486 DX, vs 486 DX/2). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DL holds minor CPU revision.
35h	Major CPU Revision Differentiates between different CPUs (i.e., 386, 486, Pentium). This is crucial for correctly determining CPU input clock frequency. During a power-on reset, Reg DH holds major CPU revision.
36h	Hotkey Usage Bits 7-6 = Reserved Bit 5 = Semaphore for Completed POST Bit 4 = Semaphore for 0 Volt POST (not currently used) Bit 3 = Semaphore for already in SCU menu Bit 2 = Semaphore for already in PM menu Bit 1 = Semaphore for SCU menu call pending Bit 0 = Semaphore for PM menu call pending
40h-7Fh	Definitions for these locations vary depending on the chipset.

3.5. EEPROM saved CMOS Setup

The EEPROM has different functions, as listed below:

- Backup of the CMOS-Setup values.
- Storing system information such as: version, production date, customization of the board, CPU type.
- Storing user/application values.

The EEPROM will be updated automatically after exiting the BIOS setup menu. The system will operate also without any CMOS battery. While booting, the CMOS is automatically updated with the EEPROM values.

If the system hangs or a problem appears, the following steps must be performed:

1. Reset the CMOS-Setup (disconnect the battery for at least 10 minutes).
2. Press Esc until the system starts up.
3. Enter the BIOS Setup:
    a. load DEFAULT values
    b. enter the settings for the environment
    c. exit the setup
4. Restart the system.

- The user may access the EEPROM through the INT15 special functions. Refer to the driver/software/BIOS manual “GEODE_LX800-LX900.pdf” on the Product CD, the chapter on Special Peripherals, Subsection “INT 15h SFR Functions”.
- The system information is read-only information. To read, use the SFI functions.

3.6. PCI Resources / PCI Slot Assignment

The following LX800/900 definitions for PCI resources for peripherals corresponds with the LX800/900 BIOS. Pay attention – the AD24 is used twice and has a special transparent mode for bridge functions and to support negative/positive mode to separate the two bridges (LX internal and PCI-to-ISA). The other IDSELs are not defined and need a customized PCI Table BIOS.

Device	IDSEL	PIRQ	REQ#/GNT#* In the BIOS	REQ#/GNT# at the SM800-bus	Comments
External on motherboard			**Informational purpose only**	**Important for Design-In**	
SLOT 1	AD20	A, B, C, D	3	0	For external use
SLOT 2	AD21	B, C, D, A	4	1	For external use
SLOT 3	AD22	C, D, A, B	5	2	For external use
SLOT 4	AD23	D, A, B, C	6	3	For external use
Internal in the SM800PCX					
LAN controller	AD29	A	7		LAN on-module (only on PCX)
PCI-ISA bridge	AD24-	--	8		PCI to ISA bridge on-module
LX-ISA bridge	AD24+		8		GEODE internal ISA comp.
CS5536	AD25	---	2		For VGA, IDE and USB
Arbiter 0	---	---	0		On-module USB
Arbiter 1	---	---	1		On-module REQ/GNT-Expander
	AD28				Reserved
	AD27				Reserved
	AD26				Reserved
	AD30				Reserved
	AD31				Reserved

AD24 with special features to support positive and negative transparent bridges.

Example:

For a motherboard with PCI frame grabber, SATA controller and PCI-to-PCI bridge, it is recommended to use:

Device	IDSEL	PIRQ	REQ#/GNT# at the SM800-bus	Comments
External on motherboard				
1st PCI controller frame grabber	AD20	A	0	BT878
2nd PCI controller PCI to PCI bridge	AD21		1	Intel PCI2050
3rd PCI controller SATA controller	AD22	C	2	SATA controller
4th PCI controller xy	AD23	D	3	As an example

Recommended (for debug purposes):

Place a 0 Ohm resistor in each IDSEL and REQx/GNTx line. This allows changing the PCI resource in the final PCB.

3.7. Memory & I/O Map

3.7.1. System Memory Map

The Geode™ CPU, used as central processing unit, has a memory address space which is defined by 32 address bits. Therefore, it can address 1 GByte of memory. The memory address map is as follows:

CPU Geode LX800 / LX900

Address:	Size:	Function / Comments:
000000 - 09FFFFh	640KByte	Onboard DRAM for DOS applications
0A0000 - 0BFFFFh	128KByte	CGA, EGA, LCD Video RAM 128kB
0C0000 - 0C8FFFh 0C9000 - 0CFFFFh	32KByte 32KByte	BIOS and VGA BIOS extensions
0D0000 - 0D4000h 0D4000 - 0D8000h 0D8000 - 0DFFFFh	16KByte 16KByte 32KByte	Free for user Free for user Free for user
0E0000 - 0EFFFFh	64KByte	Core BIOS selected by the CS5536 chipset
0F0000 - 0FFFFFh	64KByte	Core BIOS selected by the CS5536 chipset
100000 - 1FFFFFh	1MByte	DRAM for extended onboard memory
200000 - FFFFFFh	14MByte	DRAM for extended onboard memory

3.7.2. System I/O Map

The following table details the legacy I/O range for 000h through 4FFh. Each I/O location has a read/write (R/W) capability.

Note the following abbreviations:

---	Unknown or can not be determined.
Yes	Read and write the register at the indicated location. No shadow required.
WO	Write only. Value written can not be read back. Reads do not contain any useful information.
RO	Read only. Writes have no effect.
Shw	The value written to the register can not be read back via the same I/O location. Read back is accomplished via a “Shadow” register located in MSR space.
Shw@	Reads of the location return a constant or meaningless value.
Shw$	Reads of the location return a status or some other meaningful information
Rec	Writes to the location are “recorded” and written to the LPC. Reads to the location return the recorded value. The LPC is not read.

I/O Map

I/O Addr.	Function	Size	R/W	Comment
000h	Slave DMA Address - Channel 0	8bit	Yes	16bit values in two transfers.
001h	Slave DMA Counter - Channel 0	8bit	Yes	16bit values in two transfers.
002h	Slave DMA Address - Channel 1	8bit	Yes	16bit values in two transfers.
003h	Slave DMA Counter - Channel 1	8bit	Yes	16bit values in two transfers.
004h	Slave DMA Address - Channel 2	8bit	Yes	16bit values in two transfers.
005h	Slave DMA Counter - Channel 2	8bit	Yes	16bit values in two transfers.
006h	Slave DMA Address - Channel 3	8bit	Yes	16bit values in two transfers.
007h	Slave DMA Counter - Channel 3	8bit	Yes	16bit values in two transfers.
008h	Slave DMA Command/Status - Channels [3:0]	8bit	Shw$	
009h	Slave DMA Request - Channels [3:0]	8bit	WO	Reads return value B2h.
00Ah	Slave DMA Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Bh	Slave DMA Mode - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Ch	Slave DMA Clear Pointer - Channels [3:0]	8bit	WO	Reads return value B2h.
00Dh	Slave DMA Reset - Channels [3:0]	8bit	WO	Reads return value B2h.
00Eh	Slave DMA Reset Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
00Fh	Slave DMA General Mask - Channels [3:0]	8bit	Shw@	Reads return value B2h.
010h-01Fh	No Specific Usage	---	---	
020h	PIC Master - Command/Status	8bit	Shw$	
021h	PIC Master - Command/Status	8bit	Shw$	
022h-03Fh	No Specific Usage	---	---	
040h	PIT – System Timer	8bit	Shw$	
041h	PIT – Refresh Timer	8bit	Shw$	
042h	PIT – Speaker Timer	8bit	Shw$	
043h	PIT – Control	8bit	Shw$	
044h-05Fh	No Specific Usage	---	---	

Continued…

I/O Map *continued…*

I/O Addr.	Function	Size	R/W	Comment
060h	Keyboard/Mouse - Data Port	8bit	Yes	If KEL Memory Offset 100h[0] = 1(Emulation-Enabled bit). If MSR 5140001Fh[0] = 1 (SNOOP bit) and KEL Memory Offset 100h[0] = 0 (Emulation-Enabled bit).
061h	Port B Control	8bit	Yes	
062h-063h	No Specific Usage	---	---	
064h	Keyboard/Mouse - Command/ Status	8bit	Yes	If KEL Memory Offset 100h[0] = 1 (Emulation-Enabled bit). . If MSR 5140001Fh[0] = 1 (SNOOP bit) and KEL Memory Offset 100h[0] = 0 (Emulation-Enabled bit)
065h-06Fh	No Specific Usage	---	---	
070h-071h	RTC RAM Address/Data Port	8bit	Yes	Options per MSR 51400014h[0]. (*Note 1*)
072h-073h	High RTC RAM Address/Data Port	8bit	Yes	Options per MSR 51400014h[1].
074-077h	No Specific Usage	---	---	
078h-07Fh	No Specific Usage	---	---	
080h	Post Code Display	8bit	Rec	Write LPC and DMA. Read only DMA.
081h	DMA Channel 2 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
082h	DMA Channel 3 Low Page			
083h	DMA Channel 1 Low Page			
084h-086h	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only DMA.
087h	DMA Channel 0 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
088h	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only DMA.
089h	DMA Channel 6 Low Page	8bit	Rec	Upper addr bits [23:16]. Write LPC and DMA. Read only DMA.
08Ah	DMA Channel 7 Low Page			
08B	DMA Channel 5 Low Page			
08Ch-08Dh	No Specific Usage	8bit	Rec	Write LPC and DMA. Read only
08Eh	DMA			
08Fh	DMA C4 Low Page	8bit	Rec	Upper addr bits [23:16]. See comment at 080h.
090h-091h	No Specific Usage	---	---	
092h	Port A	8bit	Yes	If kel_porta_en is enabled, then access Port A; else access LPC.
093h-09Fh	No Specific Usage	---	---	
0A0h	PIC Slave - Command/Status	8bit	Shw$	
0A1h	PIC Slave - Command/Status	8bit	Shw$	
0A2h-0BFh	No Specific Usage	8bit	---	
0C0h	Master DMA Address - Channel 4	8bit	Yes	16bit values in two transfers.
0C1h	No Specific Usage	8bit	---	
0C2h	Master DMA Counter - Channel 4	8bit	Yes	16bit values in two transfers.
0C3h	No Specific Usage	8bit	---	
0C4h	Master DMA Address - Channel 5	8bit	Yes	16bit values in two transfers.
0C6h	Master DMA Counter - Channel 5	8bit	Yes	16bit values in two transfers.
0C7h	No Specific Usage	8bit	---	
0C8h	Master DMA Address - Channel 6	8bit	Yes	16bit values in two transfers.
0CAh	Master DMA Counter - Channel 6	8bit	Yes	16bit values in two transfers.
0CBh	No Specific Usage	8bit	---	
0CCh	Master DMA Address - Channel 7	8bit	Yes	16bit values in two transfers.

Continued…

I/O Map *continued…*

I/O Addr.	Function	Size	R/W	Comment
0CDh	No Specific Usage	8bit	---	

0CEh	Master DMA Counter - Channel 7	8bit	Yes	16bit values in two transfers.
0CFh	No Specific Usage	8bit	---	
0D0h	Master DMA Command/Status – Channels [7:4]	8bit	Shw$	
0D1h	No Specific Usage	8bit	---	
0D2h	Master DMA Request - Channels [7:4]	8bit	WO	
0D3h	No Specific Usage	8bit	---	
0D4h	Master DMA Mask - Channels [7:4]	8bit	Yes	
0D5h	No Specific Usage	8bit	---	
0D6h	Master DMA Mode - Channels [7:4]	8bit	Shw@	
0D7h	No Specific Usage	8bit	---	
0D8h	Master DMA Clear Pointer - Channels [7:4]	8bit	WO	
0D9h	No Specific Usage	8bit	---	
0DAh	Master DMA Reset - Channels [7:4]	8bit	WO	
0DBh	No Specific Usage	8bit	---	
0DCh	Master DMA Reset Mask - Channels [7:4]	8bit	WO	
0DDh	No Specific Usage	8bit	---	
0DEh	Master DMA General Mask - Channels [7:4]	8bit	Shw@	
0DFh	No Specific Usage	8bit	---	
0E0h-2E7h	No Specific Usage	---	---	
2E8h-2EFh	UART/IR - COM4	8bit	---	MSR bit enables/disables into I/O 2EFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
2F0h-2F7h	No Specific Usage	---	---	
2F8h-2FFh	UART/IR - COM2	8bit	---	MSR bit enables/disables into I/O 2FFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
300h- 36Fh	No Specific Usage	---	---	
370h	Floppy Status R A	8bit	RO	Second Floppy.
371h	Floppy Status R B	8bit	RO	Second Floppy.
372h	Floppy Digital Out	8bit	Shw@	Second Floppy.
373h	No Specific Usage	8bit	---	
374h	Floppy Cntrl Status	8bit	RO	Second Floppy.
375h	Floppy Data	8bit	Yes	Second Floppy.
376h	No Specific Usage	8bit	---	
377h	Floppy Conf Reg	8bit	Shw$	Second Floppy.
378h-3E7h	No Specific Usage	---	---	
3E8h-3EFh	UART/IR - COM3	8bit	---	MSR bit enables/disables into I/O 3EFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
3F0h	Floppy Status R A	8bit	RO	First Floppy.
3F1h	Floppy Status R B	8bit	RO	First Floppy.
3F2h	Floppy Digital Out	8bit	Shw@	First Floppy.

Continued…

I/O Map *continued…*

I/O Addr.	Function	Size	R/W	Comment
3F3h	No Specific Usage	8bit	---	
3F4h	Floppy Cntrl Status	8bit	RO	First Floppy.
3F5h	Floppy Data	8bit	Yes	First Floppy.

3F6h	No Specific Usage	8bit	---	
3F7h	Floppy Conf Reg	8bit	Shw$	First Floppy.
3F8h-3FFh	UART/IR - COM1	8bit	---	MSR bit enables/disables into I/O 3FFh space. (UART1 MSR 51400014h[18:16], UART2 MSR 51400014h[22:20]). Defaults to LPC.
480h	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
481h	DMA Channel 2 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
482h	DMA Channel 3 High Page			
483h	DMA Channel 1 High Page			
484h-486h	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
487h	DMA Channel 0 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
489h	DMA Channel 6 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
48Ah	DMA Channel 7 High Page			
48Bh	DMA Channel 5 High Page			
48Ch-48Eh	No Specific Usage	8bit	WO	Write LPC and DMA. Read only DMA.
48Fh	DMA Channel 4 High Page	8bit	Rec	Upper addr bits [31:24]. Write LPC and DMA. Read only DMA.
490h-4CFh	No Specific Usage	---	---	
4D0h	PIC Level/Edge	8bit	Yes	IRQ0-IRQ 7.
4D1h	PIC Level/Edge	8bit	Yes	IRQ8-IRQ15.
4D2h-4FFh	No Specific Usage	---	---	

3.8. BIOS Data Area Definitions

The BIOS Data Area is a region within the system RAM that contains information about the system environment. System environment information includes definitions associated with hard disks, diskette drives, keyboard and video, as well as other BIOS functions. This area is created when the system is first powered on and occupies a 256Byte area from 0400h-04FFh. The following table lists the contents of the BIOS data area locations in offset order starting from segment address 40:00h.

Location	Description
00h-07h	I/O addresses for up to 4 serial ports
08h-0Dh	I/O addresses for up to 3 parallel ports
0Eh-0Fh	Segment address of extended data address
10h-11h	Equipment list Bits 15-14 = Number of parallel printer adapters 00 = Not installed 01 = One 10 = Two 11 = Three Bits 13-12 = Reserved Bits 11-9 = Number of serial adapters 00 = Not installed 001 = One 010 = Two 011 = Three 100 = Four Bit 8 = Reserved Bits 7-6 = Number of diskette drives 00 = One drive 01 = Two drives Bits 5-4 = Initial video mode 00 = EGA or PGA 01 = 40 x 25 color 10 = 80 x 25 color 11 = 80 x 25 monochrome Bit 3 = Reserved Bit 2 = (1) Pointing device present Bit 1 = (1) Math coprocessor present Bit 0 = (1) Diskette drive present
12h	Reserved for port testing by manufacturer Bits 7-1 = Reserved Bit 0 = (0) Non-test mode (1) Test mode
13h	Memory size in kilobytes - low byte
14h	Memory size in kilobytes - high byte
15h-16h	

Continued...

BIOS Data Area Definitions *continued...*

Location	Description
15h-16h	Reserved
17h	Keyboard Shift Qualifier States Bit 7 = Insert mode , Bit 6 = CAPS lock Bit 5 = Num Lock, Bit 4 = Scroll Lock Bit 3 = Either Alt key, Bit 2 = Either Control key Bit 1 = Left Shift key Bit 0 = Right shift key (0 = not set / 1 = set)
18h	Keyboard Toggle Key States Bit 7 = (1) Insert held down Bit 6 = (1) CAPS lock held down Bit 5 = (1) Num Lock held down Bit 4 = (1) Scroll Lock held down Bit 3 = (1) Control+Num Lock held down Bit 2 = (1) Sys Re held down Bit 1 = (1) Left Alt held down Bit 0 = (1) Left Control held down
19h	Scratch area for input from Alt key and numeric keypad
1Ah-1Bh	Pointer to next character in keyboard buffer
1Ch-1Dh	Pointer to last character in keyboard buffer
1Eh-3Dh	Keyboard Buffer: consists of 16 word entries
3Eh	Diskette Drive Recalibration Flag Bit 7 = (1) Diskette hardware interrupt occurred Bits 6-4 = Not used Bits 3-2 = Reserved Bit 1 = (0) Recalibrate drive B Bit 0 = (0) Recalibrate drive A
3Fh	Diskette Drive Motor Status Bit 7 = Current operation 0 = Write or Format 1 = Read or Verify Bit 6 = Reserved Bits 5-4 = Drive Select 00 = Drive A 01 = Drive B Bits 3-2 = Reserved 0 = Disable / 1 = Enabled Bit 1 = Drive B Motor Status 0 = Off / 1 = On Bit 1 = Drive A Motor Status 0 = Off / 1 = On

Continued…

BIOS Data Area Definitions *continued...*

Location	Description
40h	Diskette Drive Motor Timeout Disk drive motor is powered off when the value via the INT 08h timer interrupt reaches 0.
41h	Diskette Drive Status Bit 7 = Drive Ready 0 = Ready / 1 = Not ready Bit 6 = Seek Error 0 = No error / 1 = Error occurred Bit 5 = Controller operation 0 = Working / 1 = Failed Bits 4-0 = Error Codes 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 06h = Diskette change line active (door opened) 08h = DMA overrun error 09h = Data boundary error 0Ch = Unknown media type 10h = ECC or CRC error 20h = Controller failure 40h = Seek operation failure 80h = Timeout
42h-48h	Diskette Controller Status Bytes
49h	Video Mode Setting
4Ah-4Bh	Number of Columns on screen
4Ch-4Dh	Size of Current Page, in Bytes
4Eh-4Fh	Address of Current Page
50h-5Fh	Position of cursor for each video page. Current cursor position is stored two Bytes per page. First Byte specifies the column; the second Byte specifies the row.
60h-61h	Start and end lines for 6845-compatible cursor type. 60h = starting scan line, 61h = ending scan line
62h	Current Video Display Page
63h-64h	6845-compatible I/O port address for current mode 3B4h = Monochrome 3D4h = Color
65h	Register for current mode select
66h	Current palette setting
67-6Ah	Address of adapter ROM
6Bh	Last interrupt the occurred
6Ch-6Dh	Low word of timer count

Continued…

BIOS Data Area Definitions *continued...*

Location	Description
6Eh-6Fh	High word of timer count
70h	Timer count for 24-hour rollover flag
71h	Break key flag
72h-73h	Reset flag 1243h = Soft reset. Memory test is bypassed.
74h	Status of last hard disk operation 00h = No error 01h = Invalid function requested 02h = Address mark not located 03h = Write protect error 04h = Sector not found 05h = Reset failed 08h = DMA overrun error 09h = Data boundary error 0Ah = Bad sector flag selected 0Bh = Bad track detected 0Dh = Invalid number of sectors on format 0Eh = Control data address mark detected 0Fh = DMA arbitration level out of range 10h = ECC or CRC error 11h = Data error corrected by ECC 20h = Controller failure 40h = Seek operation failure 80h = Timeout AAh = Drive not ready BBh = Undefined error occurred CCh = Write fault on selected drive E0h = Status error or error register = 0 FFh = Sense operation failed
75h	Number of hard drives
76h-77h	Work area for hard disk
78h-7Bh	Default parallel port timeout values
7Dh-7Fh	Default serial port timeout values
80h-81h	Pointer to start of keyboard buffer
82h-83h	Pointer to end of keyboard buffer
84h-88h	Reserved for EGA/VGA BIOS
8Ah	Reserved

Continued…

BIOS Data Area Definitions *continued...*

Location	Description
8Bh	Diskette drive data transfer rate information Bits 7-5 = Data rate on last operation 00 = 500 kBS 01 = 300 kBS 10 = 250 kBS Bits 5-4 = Last drive step rate selected Bits 3-2 = Data transfer rate at start of operation 00 = 500 kBS 01 = 300 kBS 10 = 250 kBS Bits 1-0 = Reserved
8Ch	Copy of hard status register
8Dh	Copy of hard drive error register
8Eh	Hard drive interrupt flag
8Fh	Diskette controller information Bit 7 = Reserved Bit 6 = (1) Drive confirmed for drive B Bit 5 = (1) Drive B is multi-rate Bit 4 = (1) Drive B supports line change Bit 3 = Reserved Bit 2 = (1) Drive determined for drive A Bit 1 = (1) Drive B is multi-rate Bit 0 = (1) Drive B supports line change
90h-91h	Media type for drives Bits 7-6 = Data transfer rate 00 = 500 kBS / 01 = 300 kBS / 10 = 250 kBS Bit 5 = (1) Double stepping required when 360k diskette inserted into 1.2MB drive Bit 4 = (1) Known media is in drive Bit 3 = Reserved Bits 2-0 = Definitions upon return to user applications 000 = Testing 360k in 360k drive 001 = Testing 360k in 1.2MB drive 010 = Testing 1.2MB in 1.2MB drive 011 = Confirmed 360k in 360k drive 100 = Confirmed 360k in 1.2MB 101 = Confirmed 1.2MB in 1.2MB drive 111 = 720k in 720k drive or 1.44MB in 1.44MB drive
92h-93h	Scratch area for diskette media. Low Byte for drive A, high Byte for drive B.
94h-95h	Current track number for both drives. Low Byte for drive A, high Byte for drive B.

Continued…

BIOS Data Area Definitions *continued...*

Location	Description
96h	Keyboard Status Bit 7 = (1) Read ID Bit 6 = (1) Last code was first ID Bit 5 = (1) Force to Num Lock after read ID Bit 4 = (1) Enhanced keyboard installed Bit 3 = (1) Right ALT key active Bit 2 = (1) Right Control key active Bit 1 = (1) Last code was E0h Bit 0 = (1) Last code was E1h
97h	Keyboard Status Bit 7 = (1) Keyboard error Bit 6 = (1) Updating LEDs Bit 5 = (1) Resend code received Bit 4 = (1) Acknowledge received Bit 3 = Reserved Bit 2 = (1) Caps Lock LED state Bit 1 = (1) Num Lock LED state Bit 0 = (1) Scroll Lock LED state
98h - 99h	Offset address of user wait flag
9Ah - 9Bh	Segment address of user wait flag
9Ch - 9Dh	Wait count, in microseconds (low word)
9Eh - 9Fh	Wait count, in microseconds (high word)
A0h	Wait active flag Bit 7 = (1) Time has elapsed Bits 6-1 = Reserved Bit 0 = (1) INT 15h, AH = 86h occurred
A1h - A7h	Reserved
A8h - ABh	Pointer to video parameters and overrides
ACh - FFh	Reserved
100h	Print screen status byte

3.8.1. Compatibility Service Table

In order to ensure compatibility with industry-standard memory locations for interrupt service routines and miscellaneous tabular data, the BIOS maintains tables and jump vectors.

Location	Description
FE05Bh	Entry Point for POST
FE2C3h	Entry point for INT 02h (NMI service routine)
FE3FEh	Entry point for INT 13h (Diskette Drive Services)
FE401h	Hard Drive Parameters Table
FE6F1h	Entry point for INT 19h (Bootstrap Loader routine)
FE6F5h	System Configuration Table
FE739h	Entry point for INT 14h (Serial Communications)
FE82Eh	Entry point for INT 16h (Keyboard Services)
FE897h	Entry point for INT 09h (Keyboard Services)
FEC59h	Entry point for INT 13h (Diskette Drive Services)
FEF57h	Entry point for INT OEh (Diskette Hardware Interrupt)
FEFC7h	Diskette Drive Parameters Table
FEFD2h	Entry point for INT 17h (Parallel Printer Services)
FF065h	Entry point for INT 10h (CGA Video Services)
FF0A4h	Video Parameter Table (6845 Data Table - CGA)
FF841h	Entry point for INT 12h (Memory Size Service)
FF84Dh	Entry point for INT 11h (Equipment List Service)
FF859h	Entry point for INT 15h (System Services)
FFA6Eh	Video graphics and text mode tables
FFE6Eh	Entry point for INT 1Ah (Time-of-Day Service)
FFEA5h	Entry Point for INT 08h (System Timer Service)
FFEF3h	Vector offset table loaded by POST
FFF53h	Dummy Interrupt routine IRET Instruction
FFF54h	Entry point for INT 05h (Print Screen Service)
FFFF0h	Entry point for Power-on
FFFF5h	BIOS Build Date (in ASCII)
FFFFEh	BIOS ID

3.9. VGA / LCD Controller

3.9.1. VGA/LCD Controller of the Geode LX800 / LX900

- Highly integrated flat panel and CRT GUI Accelerator & Multimedia Engine, Palette/DAC, Clock Synthesizer, and integrated frame buffer
- HiQColor™ Technology implemented with TMED (Temporal Modulated Energy Distribution)
- Hardware Windows Acceleration
- Hardware Multimedia Support
- High-Performance flat panel display resolution and color depth at 3.3V
- 18/24bit direct interface to color TFT panels (X1)
- Advanced Power Management minimizes power usage in:
    - Normal operation
    - Standby (Sleep) modes
    - Panel-Off Power-Saving Mode
- VESA standards supported
- Fully compatible with IBM® VGA
- Driver support for Windows XP, Windows 2000

3.9.2. Graphic Modes

Bios settings: 254MB video memory (shared)

Resolution	Col. Dept.	Frequency
800x600	16bit / 32bit	60Hz – 100Hz
1024x768	16bit / 32bit	60Hz – 100Hz
1152x864	16bit / 32bit	60Hz – 100Hz
1280x1024	16bit / 32bit	60Hz – 100Hz
1600x1200	16bit / 32bit	60Hz – 100Hz
1920x1440	16bit / 32bit	60Hz – 85Hz

3.9.3. Flat Panel Functional Description

LCD Interface:

The flat panel (FP) interfaces directly to an industry standard 18bit or 24bit active matrix thin-film-transistor (TFT).

The digital RGB or video data that is supplied by the video logic is converted into a suitable format to drive a wide variety range of panels with variable bits.

The LCD interface includes dithering logic to increase the apparent number of colors displayed for use on panels with less than 6bits per color. The LCD interface also supports an automatic power sequence of panel power supplies.

Mode Selection:

The FP can be configured for operation with most standard TFT panels in the BIOS setup:

It supports TFT panels with an 18 or 24bit interface and pixel resolutions of 320x240, 640x480, 800x600, 1024x768, 1280x1024, and 1600x1200. Either one or two pixels per clock is supported for all resolutions.

For TFT panel support, the output from the dither block is directly fed to the panel data pins (DRGBx). The data that is being sent to these pins is in sync with the TFT timing signals such as HSYNC, VSYNC, and LDE.

One pixel (or two pixels in 2 px/clk mode) is shifted on every positive edge of the clock as long as DISP_ENA is active.

Enter the BIOS with F1

- Select C (Motherboard Device Configuration)
- Select F (Video and Flat panel Configuration
- Output Display = Flat Panel
  - Flat Panel Configuration
    - TYPE = TFT
      - Resolution = 320x240, 640x480, 800x600, 1024x768, 1280x1024, or 1600x1200 pixel

4. DESCRIPTION OF THE JUMPERS

4.1. The Jumpers on the SM800PC/X / SM900PC/X

Settings written in bold are defaults.

Jumper	Structure	1-2 / open	1-2 / closed
R69	DMA for ISA	**Enable**	Disable
R78	DMA for Floppy (DMA on Super I/O)	Disable	**Enable**
R82	LAN AUX (power boot strap option)	**Disable**	Enable
R110	GPIO16 (Super I/O con. to AVR)	**Disable**	Enable
R111	GPIO17 (Super I/O con. to AVR)	**Disable**	Enable
R115	WORK_AUX (connected to AVR)	**Disable**	Enable
R114	TINY_MOSI (automatically boot)	**Enable**	Disable
R92	PCI Slot 3 #GNTon SM800PC	Slave	**Master**
R92	PCI Slot 3 #GNT on SM800PCX	**Slave**	Master
R94	PCI Slot 3 #REQ on SM800PC	Slave	**Master**
R94	PCI Slot 3 #REQ on SM800PCX	**Slave**	Master

Jumper	Structure		1-2 / closed
R100	LCD Backlight enable	or	Enable
R105	LCD VDD enable		**Enable**

5. LED CRITERIA

LED	Color	Function
D8	Green	3.3V OK
D9	Green	Run OK

5.1. The Power / Control LEDs on the SM800PC/X / SM900PC/X

There are 2 LEDs located on the top side of the smartModule-800PCX.

The GREEN POWER LED D8

It indicates that the 3.3V core supply for the CPU is OK.
This LED must light, as soon as the external 5V power supply is available.

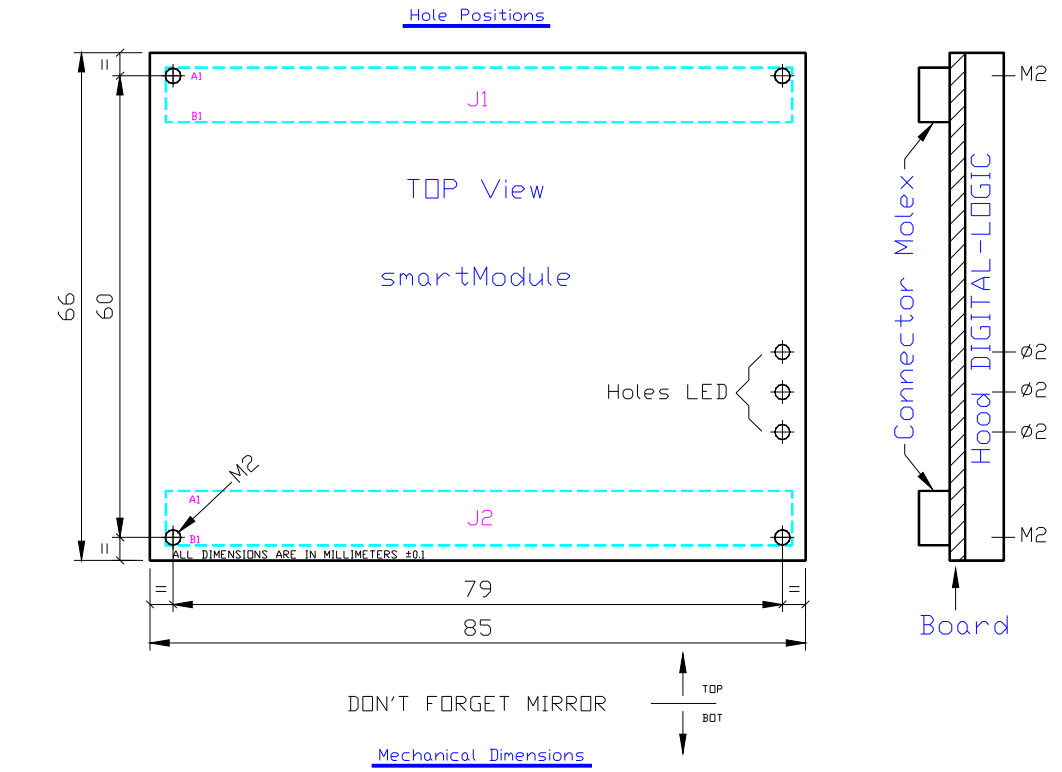
The GREEN RUN LED D9

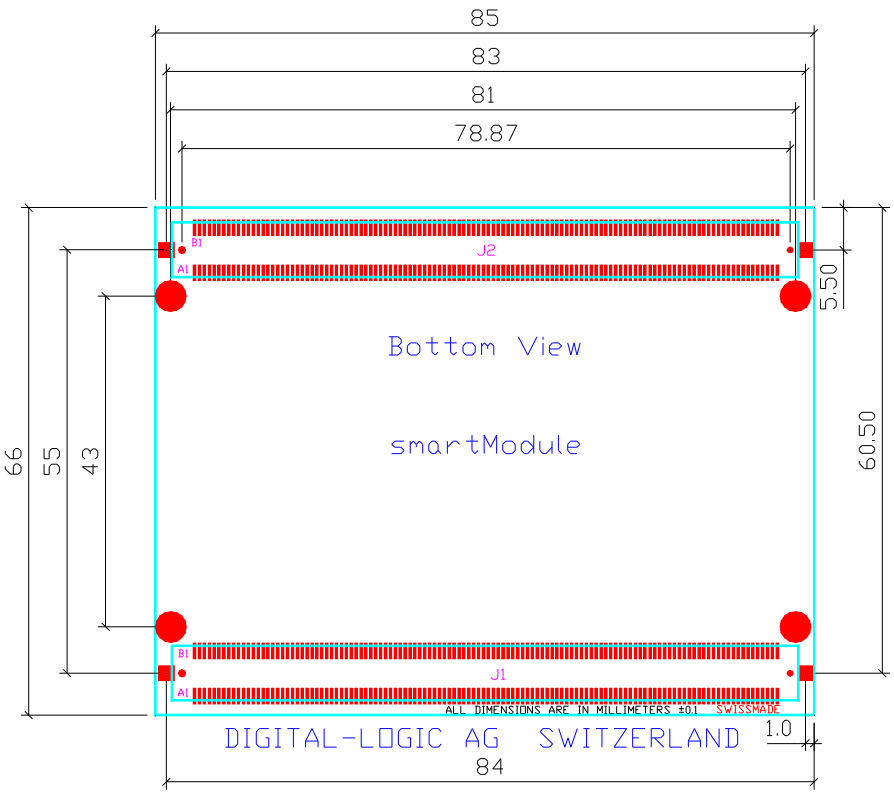
OFF: The module is in the OFF state, which means no operation.
The LED is in a flashing state.

ON: The module is in an ON state, which means it is running normally.
After power-up, this LED must turn ON after 1-2sec.

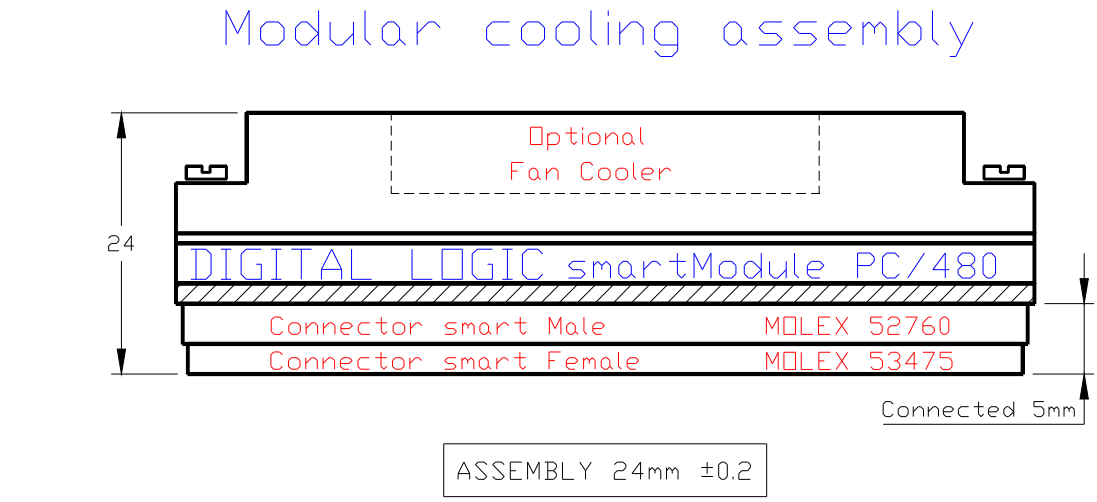
AFTER A SUCCESSFUL BOOT SEQUENCE: BOTH GREEN LEDs ARE ON!

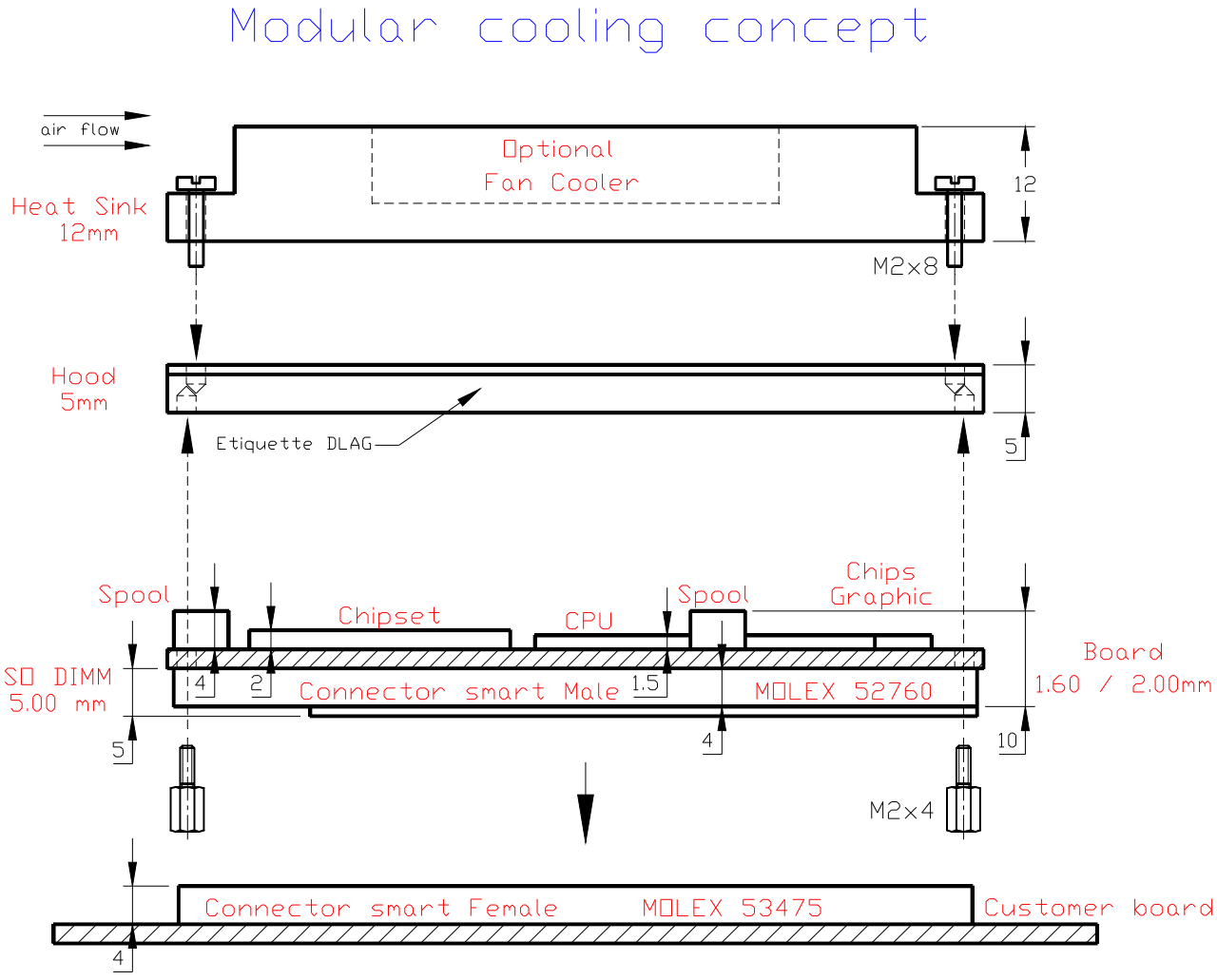
6. MECHANICAL DIMENSIONS OF THE SM800PC/X / SM900PC/X





6.1.1. PCB to SM800PC/X / SM900PC/X Height





6.2. The smart480 bus

SM800PCX Connector X200.A Pin 1-40 (J1)

Pin	Group	Volt	SM800PC	Pin	Group	Volt	SMP5PC
A1	POWER		VCC (5V)	B1			NC
A2	ISA	5 o	RESDRV	B2	ISA	5 i	IRQ2/9
A3	ISA	5 i	SBHE#	B3	ISA	5 i	IRQ3
A4	ISA	5 i	MEMCS16#	B4	ISA	5 i	IRQ4
A5	ISA	5 i	IOCS16#	B5	ISA	5 i	IRQ5
A6	ISA	5 o	IOW#	B6	I		NC
A7	ISA	5 o	IOR#	B7	ISA	5 i	IRQ7
A8	ISA	5 o	SYSCLK	B8	ISA	5 i	IRQ10
A9	ISA	5 o	TC	B9	ISA	5 i	IRQ11
A10	ISA	5 o	ALE	B10	ISA	5 i	IRQ12
A11	ISA	5 i/o	SD7	B11	ISA	5 i	IRQ14
A12	ISA	5 i/o	SD6	B12	ISA	5 i	IRQ15
A13	ISA	5 i/o	SD5	B13			NC
A14	ISA	5 i/o	SD4	B14			NC
A15	ISA	5 i/o	SD3	B15	ISA	5 o	LA21
A16	ISA	5 i/o	SD2	B16	ISA	5 o	LA20
A17	ISA	5 i/o	SD1	B17	ISA	5 o	LA19
A18	ISA	5 i/o	SD0	B18	ISA	5 o	LA18
A19	ISA	5 o	IOCHRDY	B19	ISA	5 o	LA17
A20	ISA	5 o	AEN	B20	ISA	5 i/o	SD8
A21	ISA	5 o	SA19	B21	ISA	5 i/o	SD9
A22	ISA	5 o	SA18	B22	ISA	5 i/o	SD10
A23	ISA	5 o	SA17	B23	ISA	5 i/o	SD11
A24	ISA	5 o	SA16	B24	ISA	5 i/o	SD12
A25	ISA	5 o	SA15	B25	ISA	5 i/o	SD13
A26	ISA	5 o	SA14	B26	ISA	5 i/o	SD14
A27	ISA	5 o	SA13	B27	ISA	5 i/o	SD15
A28	ISA	5 o	SA12	B28	ISA	5 i	DRQ 0
A29	ISA	5 o	SA11	B29	ISA	5 i	DRQ 1
A30	ISA	5 o	SA10	B30	ISA	5 i	DRQ 2
A31	ISA	5 o	SA9	B31	ISA	5 i	DRQ 3
A32	ISA	5 o	SA8	B32	ISA	5 i	DRQ 5
A33	ISA	5 o	SA7	B33	ISA	5 i	DRQ 6
A34	ISA	5 o	SA6	B34	ISA	5 o	OSC (14.31MHz)
A35	ISA	5 o	SA5	B35	ISA	5 o	DMA0#
A36	ISA	5 o	SA4	B36	ISA	5 o	DMA1#
A37	ISA	5 o	SA3	B37	ISA	5 o	DMA2#
A38	ISA	5 o	SA2	B38	ISA	5 o	DMA3#
A39	ISA	5 o	SA1	B39	ISA	5 o	DMA5#
A40	ISA	5 o	SA0	B40	ISA	5 o	DMA6#

** These signals (LA17-LA19) correspond with the SA17-SA19.

Remarks:
5 o = 5V output 5 i/o = 5V input/output
3 o = 3V output 3 i/o = 3V input/output

# = active low signal o.c. = open collector output NC = not connected
RES = reserved, pin function depending on the CPU

SM800PCX Connector X200.A Pin 41-80 (J1)

Pin	Group	Volt	SM800PC	Pin	Group	Volt	SM800PC
A41	TINY	3 o	TINY_SCL	B41	CORE	5 o	Speaker
A42	TINY	3 o	TINY_MISO	B42	ISA	5 i	ZWS#
A43	TINY	3 o	TINY_MOSI	B43	ISA	5 o	REF#
A44	TINY	3 o	TINY_RST	B44	ISA	5 o	MEMR#
A45	TINY	3 I	TINY_VCC_PROG	B45	ISA	5 o	SMEMR#
A46	LPC	3 o	LAD0	B46	ISA	5 o	MEMW#
A47	LPC	3 o	LAD1	B47	ISA	5 o	SMEMW#
A48	LPC	3 o	LAD2	B48	VIDEO IN	3 i/o	Reserved (VIP_VID0)
A49	LPC	3 i/o	LAD3	B49	VIDEO IN	3 i/o	Reserved (VIP_VID1)
A50	LPC	3 i/o	LFRAME#	B50	VIDEO IN	3 i/o	Reserved (VIP_VID2)
A51	LPC	3 i/o	CLK_LPC_FWH	B51	VIDEO IN	3 i/o	Reserved (VIP_VID3)
A52	LPC	3 i/o	FWH_CONTROL#	B52	VIDEO IN	3 i/o	Reserved (VIP_VID4)
A53	LPC	3 i/o	PCI_RST#	B53	VIDEO IN	3 i/o	Reserved (VIP_VID5)
A54	LAN	3 i/o	LAN_LINKLED	B54	VIDEO IN	3 i/o	Reserved (VIP_VID6)
A55	LAN	3 i/o	LAN_ACTLED	B55	VIDEO IN	3 i/o	Reserved (VIP_VID7)
A56	LAN	3 i/o	LAN_SPDLED	B56	VIDEO IN	3 i/o	Reserved (VIP_HSYNC)
A57	POWER		GROUND	B57	VIDEO IN	3 i/o	Reserved (VIP_VSYNC)
A58	LPC		SERIRQ	B58	VIDEO IN	3 i/o	Reserved (VIP_SYNC)
A59			NC	B59	VIDEO IN	3 i/o	Reserved (VIP_CLK)
A60			NC	B60	VIDEO IN	3 i/o	Reserved (VIP VID8)
A61			NC	B61	VIDEO IN	3 i/o	Reserved (VIP VID9)
A62	AC97	3 i/o	AC97_BITCLK	B62	VIDEO IN	3 i/o	Reserved (VIP VID10)
A63	AC97	3 i/o	AC97_SDIN0	B63	VIDEO IN	3 i/o	Reserved (VIP VID11)
A64	AC97	3 i/o	AC97_SDOUT	B64	VIDEO IN	3 i/o	Reserved (VIP VID12)
A65	AC97	3 i/o	AC97_SYNC	B65	VIDEO IN	3 i/o	Reserved (VIP VID13)
A66	POWER		GROUND	B66	VIDEO IN	3 i/o	Reserved (VIP VID14)
A67			NC	B67	VIDEO IN	3 i/o	Reserved (VIP VID15)
A68			NC	B68	POWER		GND
A69			NC	B69	USB2		USB_P2+
A70			NC	B70	USB2		USB_P2-
A71			NC	B71	POWER		GND
A72			NC	B72	USB3		USB_P3+
A73			NC	B73	USB3		USB_P3-
A74			NC	B74	POWER		GND
A75			NC	B75			NC
A76			NC	B76			NC
A77			NC	B77			NC
A78			NC	B78			NC
A79			NC	B79			NC
A80			NC	B80	CORE	5 o	24MHz Output

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

smartBus480 incompatibility to SMP5/P3PC

SM800PCX Connector X200.A Pin 81-120 (J1)

Pin	Group	Volt	SM800PC	Pin	Group	Volt	SM800PC
A81			NC	B81	POWER		GROUND
A82			NC	B82			NC
A83			NC	B83			NC
A84			NC	B84			NC
A85			NC	B85			NC
A86			NC	B86			NC
A87			NC	B87			NC
A88	POWER		GROUND	B88			NC
A89			NC	B89			NC
A90			NC	B90	POWER		GROUND
A91			NC	B91			NC
A92			NC	B92			NC
A93			NC	B93			NC
A94			NC	B94			NC
A95			NC	B95			NC
A96			NC	B96			NC
A97	POWER		GROUND	B97			NC
A98			NC	B98			NC
A99			NC	B99	POWER		GROUND
A100			NC	B100			NC
A101			NC	B101			NC
A102			NC	B102			NC
A103			NC	B103			NC
A104			NC	B104			NC
A105			NC	B105			NC
A106	POWER		GROUND	B106			NC
A107			NC	B107			NC
A108			NC	B108			NC
A109			NC	B109			NC
A110			NC	B110			NC
A111			NC	B111			NC
A112			NC	B112			NC
A113			NC	B113			NC
A114			NC	B114			NC
A115			NC	B115			NC
A116			NC	B116			NC
A117			NC	B117			NC
A118			NC	B118			NC
A119			NC	B119	POWER		VCC (+5V)
A120			NC	B120	POWER		VCC (+5V)

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

SM800PCX Connector X200.B Pin1-40 (J2)

Pin	Group	Volt	SM800PC	Pin	Group	Volt	SM800PC
A1	PRINTER	5 o	strobe#	B1	COM1	5 o	DCD1
A2	PRINTER	5 o	auto#	B2	COM1	5 i	DSR1
A3	PRINTER	5 o	error#	B3	COM1	5 i	RXD1
A4	PRINTER	5 o	init#	B4	COM1	5 o	RTS1
A5	PRINTER	5 o	slctin#	B5	COM1	5 o	TXD1
A6	PRINTER	5 i/o	PRINTER data 0	B6	COM1	5 i	CTS1
A7	PRINTER	5 i/o	PRINTER data 1	B7	COM1	5 o	DTR1
A8	PRINTER	5 i/o	PRINTER data 2	B8	COM1	5 i	RI1
A9	PRINTER	5 i/o	PRINTER data 3	B9	COM2	5 o	DCD2
A10	PRINTER	5 i/o	PRINTER data 4	B10	COM2	5 i	DSR2
A11	PRINTER	5 i/o	PRINTER data 5	B11	COM2	5 i	RXD2
A12	PRINTER	5 i/o	PRINTER data 6	B12	COM2	5 o	RTS2
A13	PRINTER	5 i/o	PRINTER data 7	B13	COM2	5 o	TXD2
A14	PRINTER	5 i	acknowledge#	B14	COM2	5 i	CTS2
A15	PRINTER	5 i	busy	B15	COM2	5 o	DTR2
A16	PRINTER	5 i	paper end	B16	COM2	5 i	RI2
A17	PRINTER	5 i	select	B17	FLOPPY	5 i	index
A18	KBD	5 i/o	keyboard data	B18	FLOPPY	5 o	drive select 1
A19	KBD	5 o	keyboard clock	B19	FLOPPY	5 i	disk change
A20	MOUSE	5 o	MOUSE clock	B20	FLOPPY	5 o	motor on 1
A21	MOUSE	5 i/o	MOUSE data	B21	FLOPPY	5 o	direction
A22	POWER		Ground	B22	FLOPPY	5 o	step impulse
A23	IDE	5 i/o	IDE HD 0	B23	FLOPPY	5 o	write data
A24	IDE	5 i/o	IDE HD 1	B24	FLOPPY	5 o	write gate
A25	IDE	5 i/o	IDE HD 2	B25	FLOPPY	5 i	track zero
A26	IDE	5 i/o	IDE HD 3	B26	FLOPPY	5 i	write protected
A27	IDE	5 i/o	IDE HD 4	B27	FLOPPY	5 i	read data
A28	IDE	5 i/o	IDE HD 5	B28	FLOPPY	5 o	head select
A29	IDE	5 i/o	IDE HD 6	B29	FLOPPY	5 o	drive select 0
A30	IDE	5 i/o	IDE HD 7	B30	FLOPPY	5 o	motor on 0
A31	IDE	5 i/o	IDE HD 8	B31	APM	5 i	PWRBTN
A32	IDE	5 i/o	IDE HD 9	B32	IDE-CH1	5 o	IDE_RESET#
A33	IDE	5 i/o	IDE HD 10	B33			NC
A34	IDE	5 i/o	IDE HD 11	B34	USB0	5 i/o	USB-P0+
A35	IDE	5 i/o	IDE HD 12	B35	USB0	5 i/o	USB-P0-
A36	IDE	5 i/o	IDE HD 13	B36	IDE	5 o	A 0
A37	IDE	5 i/o	IDE HD 14	B37	IDE	5 o	A 1
A38	IDE	5 i/o	IDE HD 15	B38	IDE	5 o	A 2
A39	IDE	5 o	IDE primary cs0#	B39	IDE	5 o	IORDY
A40	IDE	5 o	IDE primary cs1#	B40			

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

SM800PCX Connector X200.B Pin 41-80 (J2)

Pin	Group	Volt	Description	Pin	Group	Volt	Description
A41	PRINTER	5 o	PDACK#	B41	IrDA	3 o	IrDA TX
A42	PRINTER	5 o	PREQ	B42	IrDA	3 i	IrDA RX
A43	IDE-CH1	5 i	IRQ	B43			
A44	IDE-CH1	5 o	IOR#	B44			
A45	IDE-CH1	5 o	IOW#	B45			
A46	POWER		VCC (5V)	B46	POWER	3 i	Battery 3.0V for RTC
A47	PCI	3 i/o	AD0	B47	PCI	3 i/o	AD16
A48	PCI	3 i/o	AD1	B48	PCI	3 i/o	AD17
A49	PCI	3 i/o	AD2	B49	PCI	3 i/o	AD18
A50	PCI	3 i/o	AD3	B50	PCI	3 i/o	AD19
A51	PCI	3 i/o	AD4	B51	PCI	3 i/o	AD 20
A52	PCI	3 i/o	AD5	B52	PCI	3 i/o	AD 21
A53	PCI	3 i/o	AD6	B53	PCI	3 i/o	AD 22
A54	PCI	3 i/o	AD7	B54	PCI	3 i/o	AD 23
A55	PCI	3 i/o	AD8	B55	PCI	3 i/o	AD 24
A56	PCI	3 i/o	AD9	B56	PCI	3 i/o	AD 25
A57	PCI	3 i/o	AD10	B57	PCI	3 i/o	AD 26
A58	PCI	3 i/o	AD11	B58	PCI	3 i/o	AD 27
A59	PCI	3 i/o	AD12	B59	PCI	3 i/o	AD 28
A60	PCI	3 i/o	AD13	B60	PCI	3 i/o	AD 29
A61	PCI	3 i/o	AD14	B61	PCI	3 i/o	AD 30
A62	PCI	3 i/o	AD15	B62	PCI	3 i/o	AD31
A63	PCI	3 o	C-BE0#	B63	PCI	3 i	INTA
A64	PCI	3 o	C-BE1#	B64	PCI	3 i	INTB
A65	PCI	3 o	C-BE2#	B65	PCI	3 i	INTC
A66	PCI	3 o	C-BE3#	B66	PCI	3 i	INTD
A67	POWER		VCC (5V)	B67	POWER		VCC (5V)
A68	PCI	3 o	PCI-CLK0	B68	PCI	3 o	PCI-CLK1
A69	PCI	3 i	REQ0#	B69	PCI	3 o	GNT0#
A70	PCI	3 i	REQ1#	B70	PCI	3 o	GNT1#
A71	PCI	3 i	REQ2#	B71	PCI	3 o	GNT2#
A72	PCI	3i	REQ#3 (only SM800)	B72	PCI	3 o	GNT#3 (only SM800)
A73			NC	B73	POWER		VCC (5V)
A74	PCI	3 i/o	FRAME#	B74	PCI	3 i/o	IRDY#
A75	PCI	3 i/o	TRDY#	B75	PCI	3 i/o	STOP#
A76	PCI	3 i/o	DEVSEL#	B76	PCI	3 i/o	PAR#
A77	PCI	3 i/o	SERR#	B77	PCI	3 i/o	LOCK# = PLOCK#
A78			NC	B78	PCI	3 o	PCI-RESET#
A79	CORE	3 i	RESET#	B79	ISA	5 i	DRQ7
A80			NC	B80	ISA	5 0	DACK7

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

BIOS settings to use the IrDa:

You must enable the UART A of the GeodeLX in the bios setup:
F1 ➔ Motherboard device configuration ➔ I/O configuration:

UART port A = enabled
UART mode = SIR/CIR

ATTENTION!

Never set the UART A mode to “Serial – 16550 compatible” or “Extended” if an IrDa diode is connected to the B41/B42. ***The diode will be destroyed!***

SM800PCX Connector X200.B Pin 81-120 (J2)

Pin	Group	Volt	SM800PC	Pin	Group	Volt	SM800PC
A81			NC	B81	USB1	5 i/o	USB_P1+
A82			NC	B82	USB1	5 i/o	USB_P1-
A83			NC	B83			NC
A84			NC	B84			NC
A85			NC	B85	ISA	5 o	LA22
A86			NC	B86	ISA	5 o	LA23
A87			NC	B87	PCI	5 i/o	PERR-
A88			NC	B88	GPIO	3 i/o	GPIO30
A89	GPIO	3 i/o	GPIO31	B89	I2C	3 i/o	SMB-DAT
A90	GPIO	3 i/o	GPIO34	B90	I2C	3 o	SMB-CLK
A91	POWER		3.3V	B91	POWER		3.3V
A92	LAN	3 o	LAN_TX+	B92	ISA	5 i	MASTER#
A93	LAN	3 o	LAN_TX-	B93	ISA	5 i	IOCHCK
A94	LAN	3 i	LAN_RX+	B94	JTAG	3 i	JTAG_CLK
A95	LAN	3 i	LAN_RX-	B95	JTAG	3 i	JTAG_TDI
A96			NC	B96	JTAG	3 o	JTAG_TD0
A97	POWER		VCC_SUS	B97	JTAG	3 o	JTAG_TMS
A98	TINY	3 i/o	SUSA	B98	VGA	3 i/o	CRT_SDA
A99	TINY	3 i/o	SUSB	B99	VGA	3 o	CRT_SCL
A100	TINY	3 i/o	SUSC	B100			NC
A101	VGA	O	VGA GREEN	B101	VGA		VGA GROUND
A102	VGA	O	VGA BLUE	B102	VGA	o	VSYNC
A103	VGA	O	VGA RED	B103	VGA	o	HSYNC
A104			NC	B104	LCD	3 o	LCD_ENAVDD
A105	POWER		GROUND	B105	LCD	3 o	LCD_SHCLK
A106	LCD	3 o	VSYNC	B106	LCD	3 o	HSYNC
A107	LCD	3 o	LCD_D12	B107	LCD	3 o	LCD_D0
A108	LCD	3 o	LCD_D13	B108	LCD	3 o	LCD_D1
A109	LCD	3 o	LCD_D14	B109	LCD	3 o	LCD_D2
A110	LCD	3 o	LCD_D15	B110	LCD	3 o	LCD_D3
A111	LCD	3 o	LCD_D16	B111	LCD	3 o	LCD_D4
A112	LCD	3 o	LCD_D17	B112	LCD	3 o	LCD_D5
A113	LCD	3 o	LCD_D18	B113	LCD	3 o	LCD_D6
A114	LCD	3 o	LCD_D19	B114	LCD	3 o	LCD_D7
A115	LCD	3 o	LCD_D20	B115	LCD	3 o	LCD_D8
A116	LCD	3 o	LCD_D21	B116	LCD	3 o	LCD_D9
A117	LCD	3 o	LCD_D22	B117	LCD	3 o	LCD_D10
A118	LCD	3 o	LCD_D23	B118	LCD	3 o	LCD_D11
A119	LCD	3 o	LCD_ENABKL	B119	LCD	3 o	LCD_DE
A120	POWER		LCD_VCC (3V)	B120	POWER		VCORE

Remarks:

5 o = 5V output 5 i/o = 5V input/output

3 o = 3V output 3 i/o = 3V input/output

= active low signal o.c. = open collector output NC = not connected

7. DESIGN-IN WITH THE SMARTMODULE

PLEASE REFER TO THE SM800DK MANUAL FOR THE DESIGN-IN INFORMATION!

8. INDEX